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The Use of Selective Area Growth for the Reduction of Threading Dislocation Densities in Heteroepitaxy

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11. SUPPLEMENTARY NOTES

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13. ABSTRACT (Maximum 200 words)

The central goal of this project has been the achievement of low defect density GaAs heteroepitaxy on Si by growing mesas with free side walls. Several approaches were used singly and in combination in attempts to guide misfit dislocations (MDs) to the GaAs mesa edges and minimze threading dislocation (TD) densities. Methods included the use of Si pedestals with concave sidewalls, interposed plastically-soft ZnSe buffer layers, graded-composition InGaAs strained layers and post deposition anneals of the various structures. It was found that, surprisingly, TD densities are hardly reduced by the presence of free sidewalls. Moreover, dislocation interactions during the early stages of growth determined the structure and density of TDs in as-grown films and not thermal mismatch strain during cool down from the growth temperature. It was found that graded-strain layers led to a reduction of dislocation densities by a factor of ~15 in films grown over pedestals with convex {111} facetted sidewalls. It was concluded that to obtain minimum TD densities it is imperative to prevent formation of 90° MDs during lattice mismatched heteroepitaxial growth. The structure and thermal stability of interfaces between ZnSe and Si:As(100) were also determined. The observed asymmetric organization of dislocations was shown to arise from the formation and propagation of misfit dislocations on vicinal surfaces.

14. SUBJECT TERMS

Heteroepitaxy, Selective Area Growth, GaAs on Si

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A) Research Objectives

1. Selective area heteroepitaxy of GaAs/Si will be studied using mesas and cantilever-masked surfaces.

2. Heteroepitaxial GaAs/Si layers will be grown under various deposition conditions on planar samples with intermediate buffer layers (such as ZnSe or Ga_2Se_3) or on nonplanar samples listed above.

3. The effects of *in situ* and post-growth anneal cycles on threading dislocations will be studied using TEM and/or etch pit/ SEM analysis.

4. Growth modes will be studied using XPS, STM, LEED and TEM; correlations will be sought with dislocation nucleation and interaction.

5. Other heteroepitaxial systems than GaAs/Si will be studied as described for the purpose of comparison.

B) Summary of Research

We have studied the mechanisms that determine the density and structure of threading dislocations in GaAs on Si by growing GaAs films on continuous Si substrates and on 10-34µm wide Si pedestals. Pedestals with concave sidewalls allowed free sidewall growth of the GaAs overlayer. We also used pedestals having convex {111} facetted walls which allowed continuous film growth over the inhomogeneous features. GaAs was also grown on vicinal Ge(100) substrates as a reference to demonstrate the absence of deposition artifacts which could mask the fundamental physical effects. The dislocation structures were studied using large area, high resolution transmission electron microscopy. The results indicated that dislocation interactions during the early stages of growth determine the structure and density of TDs in as-grown films. It was also concluded that plastic relaxation of thermal mismatch strain during cool down from the growth temperature is not the principal determinant of the TD density in the films. This is in contradiction to an influential report in the literature. It was also found that interposed graded strained layers led to a reduction of dislocation density by a factor of ~5 in films grown both on mesas with concave sidewalls and on unpatterned substrates with an additional factor of 3 reduction when the convex mesas were used. The basic conclusion of the research is that, in order to obtain minimum TD density during lattice mismatched heteroepitaxial growth, contrary to the conventional wisdom, it is imperative to prevent formation of 90° misfit dislocations.

Research also focussed on the structure and stability of the interface between ZnSe and vicinal Si(100):As. High resolution electron microscopy of the as-grown films showed abrupt interfaces with an asymmetry of the misfit dislocation network at the interface relative to the substrate tilt direction. In images taken with the electron beam parallel to the [1-10] direction (perpendicular to the surface tilt axis), 60° dislocations were found to predominate, whereas

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mostly Lomer dislocations or closely spaced 60° dislocations (separated by < 2nm) were observed in images taken in the orthogonal direction. Rapid thermal annealing experiments were carried out to study the thermal stability of the ZnSe/Si:As interface at temperatures up to 960°C. The interfacial structure remained unchanged for anneals up to 800°C. Roughening of the interface was observed at 850°C. After an anneal at 900°C the interface developed a facetted structure with {111} oriented sidewalls that extended preferentially in the [1-10] direction. The 60° dislocations that were previously observed along this direction combined into closely spaced pairs or into Lomer dislocations which were associated with the facets. Models were developed both for the development of the initial asymmetric dislocation structure (on the basis of mechanisms for propagation and formation of misfit dislocations) and for the atomic structure of the facetted interface.

C)   Publications

D. K. Biegelsen, R. D. Bringans, J. E. Northrup and L.-E. Swartz, "Selenium and tellurium terminated GaAs(100) surfaces observed by scanning tunneling microscopy," Phys. Rev. B 49, 5424-5428 (1994).

R. D. Bringans, D. K. Biegelsen, L.-E. Swartz, F. A. Ponce and J. C. Tramontana, "Use of ZnSe as an Interlayer for GaAs Growth on Si," Appl. Phys. Lett. 61, 195-197 (1992).

J. Knall, L.T. Romano, D.K. Biegelsen, and R.D. Bringans, "Threading dislocation densities in GaAs grown on reduced area Si substrates," Mat. Res. Soc. Symp. Proc. 308, 417-422 (1993).

J. Knall, L. T. Romano, B. S. Krusor, D. K. Biegelsen and R. D. Bringans, "Threading dislocations in GaAs grown with free sidewalls on Si mesas'" submitted to Journal of Vacuum Science and Technology.

J. Knall, L. T. Romano, D. K. Biegelsen, R. D. Bringans, H. C. Chui, J. S. Harris, Jr., D. W. Treat and D. P. Bour, "The use of graded InGaAs layers and patterned substrates to remove threading dislocations from GaAs on Si," submitted to J. Appl. Phys.

L. T. Romano, R. D. Bringans, J. Knall, D. K. Biegelsen, A. Garcia, J. E. Northrup, and M. A. O'Keefe "Atomic rearrangement at the interface of annealed ZnSe films grown on vicinal Si(001) substrates," submitted to Phys. Rev. B.

L. T. Romano, J. Knall, R. D. Bringans and D. K. Biegelsen, "Misfit dislocations in ZnSe grown on vicinal Si (001) substrates," submitted to Appl. Phys. Letters.

Copies of the above listed papers are appended to this report

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D) Professional Personnel Associated with Project

David Biegelsen   Principal Investigator
Ross Bringans   Principal Investigator
Johan Knall   Visiting Scientist
Brent Krusor   Technical Support
Linda Romano   Visiting Scientist
Lars Swartz   Technical Support
Don Yingling *(deceased)*   Technical Support

E) Interactions

Services:

Transmission electron microscopic observations of ZnS films grown on bare and As-terminated Si for the NanoFAB Center at Texas A&M University (Wiley Kirk).

Talks at conferences:

D. K. Biegelsen, R. D. Bringans, L. Romano and L.-E. Swartz, "GaAs on Si with ZnSe Buffer Layer," American Physical Society, Indiannapolis IN March 19, 1992.

R. D. Bringans, D. K. Biegelsen, L.-E. Swartz, F. A. Ponce, J. C. Tramontana and L. Romano, "Growth of GaAs on Si with a ZnSe Buffer Layer," Materials Research Society, San Francisco, CA April 28, 1992.

R. D. Bringans, D. K. Biegelsen, L. T. Romano and L.-E. Swartz, "MBE growth modes of GaAs on Si via ZnSe interlayers," Invited talk, Conference on Physics of Compound Semiconductor Interfaces, Williamsburg, VA January 26, 1993.

R. D. Bringans, D. K. Biegelsen, L. T. Romano and L.-E. Swartz, "Growth of ZnSe on Si" Invited talk, American Physical Society March Meeting, Seattle, WA, March 24, 1993.

D. K. Biegelsen, R. D. Bringans, J. E. Northrup and L.-E. Swartz, "Atomistic processes in heteroepitaxial growth on siliicon," American Physical Society, Seattle WA, March 25, 1993.

J. Knall, L.T. Romano, D. K. Biegelsen, and R.D. Bringans, Threading dislocation densities in GaAs grown on reduced area Si substrates. Materials Research Society, San Francisco, CA April 1993.

J. Knall, L.T. Romano, D. K. Biegelsen, and R.D. Bringans, "A Study of threading dislocations in GaAs grown on reduced area Si substrates," presented at American Vacuum Society meeting in Orlando November 15-19, 1993.

R.D. Bringans, L.T. Romano, D. K. Biegelsen and J. Knall, "Atomic rearrangement at the interface formed by ZnSe Growth on Si," presented at American Vacuum Society meeting in Orlando November 15-19, 1993.

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November 17, 1993

Dr. Ross D. Bringans
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3333 Coyde Hill Rd.
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Dear Dr. Bringans:

Thank you for offering your help in TEM analysis of our ZnS/Si samples. Enclosed are four samples for the TEM analysis. Among them, S043 is a 1500Å ZnS/Si(111), S044 is a 6500 Å Zn/As/Si(111), S048 is a 3000 Å ZnS/As/Si(100)-4° off towards [011], and S054 is a 2700 Å ZnS/Si(100)-4° off towards [011]. The thicknesses that I list here are estimated values.

Also enclosed is an AFM image of a Si(111) surface after being chemically etched by using peroxide cleaning procedure and being thermally annealed at 870°C. This is the best surface that we can currently get with our present facility. Some of our samples could have surface defect densities ten times higher. I just want you to be aware of this fact so that not to be misled by seeing some strange defects. We are currently in the process of upgrading our water purification system which, we think, was a major source of our substrate contamination. Hopefully, we can decrease our surface defect density to a reasonable level in the near future.

In this work of growing ZnS on silicon surfaces, we have been inspired by many of your previous results in the related areas. I would like to, on the behalf of Prof. Wiley P. Kirk who is the director of the NanoFAB Center, express our interest of seeking a possibility of future collaboration or exchanging information with you. I enclosed a description about the research activities in our center for your reference. I will send a manuscript about our work on ZnS/Si to you in about a week.

Thank you for your interest in our work.

Sincerely yours,

Joe Xiaochuan Zhou, Ph.D.
Research Specialist

Selenium- and tellurium-terminated GaAs(100) surfaces observed by scanning tunneling microscopy

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(Received 29 September 1993)

GaAs(100) surfaces with adsorbed Se or Te have been studied using scanning tunneling microscopy (STM), x-ray-photoemission spectroscopy (XPS), and electron diffraction. STM reveals uniform dimerization which is consistent with the 2×1 symmetry of the electron diffraction. XPS shows an initial single-monolayer coverage of Se followed by a slow Se uptake which predominantly replaces As. Narrow single- and double-bilayer high islands, which are long in the [011] direction of dimer rows, are generally observed as well as terrace edges which show related kink anisotropy. Possible surface structures are discussed.

In the past few years several potentially useful aspects of the interaction between group-VI atoms, such as sulfur, and III-V compound semiconductors, such as GaAs, have been observed. Of course, the mixed oxide skin, which is formed on the surface of chemically cleaned GaAs, is one case which has been very familiar to semiconductor researchers for many years. The oxides, formed at quite low temperatures, are strongly diffusion limited in thickness to a few nm. The new findings concerning other group-VI elements are related to the passivation of surfaces[1-3] and interfaces[4,5] by sulfur and selenium, and the possible "surfactant" nature of Te on strained-layer heteroepitaxial growth of InAs on GaAs.[6] Understanding of the mechanisms underlying these important applications has been hampered due to incomplete knowledge of the structure of the chalcogenide layers. The primary probes that have been used to date to determine the structure of the chalcogenide layers have been electron diffraction and photoemission. Scanning tunneling microscopy (STM) has been a very useful, complementary tool to provide real-space information about the surface structure of semiconductors, and GaAs in particular. In this paper, we present STM images along with results of x-ray-photoemission spectroscopy (XPS) and electron diffraction of GaAs(100):Se and GaAs(100):Te surfaces. We then discuss the implications for models of the structure of these surfaces.

GaAs samples were cut from Zn-doped and Si-doped on-axis (100) wafers, solvent cleaned, etched in ultrasonified H_2SO_4, and oxidized in air under ultraviolet illumination. The samples were clipped to molybdenum holders, which incorporated radiation heater filaments sandwiched between boron nitride diffusers. Samples were baked in ultrahigh vacuum (UHV) for at least 2 h at 500 °C before oxide desorption. Buffer layers approximately 100-nm thick of nominally undoped GaAs were grown under As-rich conditions. After growth, reflection high-energy electron-diffraction (RHEED) patterns were a 2×4 array of narrow elongated spots lying on the principal arcs. The diffraction usually showed strong Kikuchi scattering and low diffuse background. The samples were cooled in an As_4 flux and held at ~ 30 °C until the As_4 pressure was $< 10^{-9}$ Torr. The chalcogen-source

Knudsen cell was then heated. Before opening the shutter, the sample was heated to a temperature of 500–600 °C to provide an initial surface stoichiometry corresponding to surface reconstructions ranging from $c(4 \times 4)$ (As rich) to 4×2 (Ga rich). The shutter was then opened and the fluence monitored with a cooled quartz crystal monitor.

Takatani, Kikawa, and Nakazawa[7] have observed in RHEED a surface reconstruction "phase diagram" for a range of molecular Se vapor pressure and substrate temperatures. We have confirmed their results that, independent of the initial clean-GaAs reconstruction, one can reversibly move from a sharp 2×1 Se-induced surface structure at high net Se arrival rates (Se flux-Se reevaporation) to a more disordered 4×3 structure at low net arrival rates, to an As-deficient bare GaAs surface. At highest net fluxes, an a-Se layer is deposited. There is a large heat of formation liberated in converting the III-V solid and group-VI molecular vapors into the respective III_2VI_3 (or III_1VI_1) and V_2VI_3 chalcogenides. GaAs should thus, in equilibrium be completely consumed by a reservoir of the group-VI species. GaAs has, in fact, been largely converted to Ga_2Se_3 by heating in a vapor of
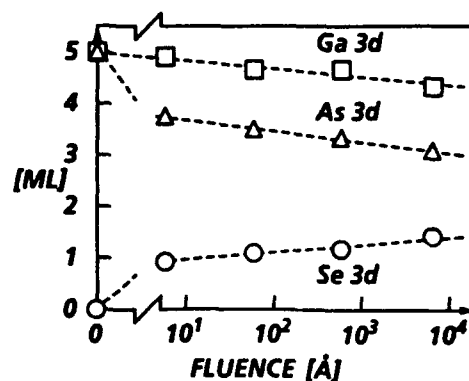

FIG. 1. Plot of measured XPS integrated peaks for Ga, As, and Se $3d$ core levels. The data have been converted to effective ML's of coverage by comparison with data for As-terminated Si(100)—known to be within 5% of 1 ML—and using calculated cross-section ratios. Upper bounds on systematic errors in coverage and fluence are estimated to be 25%.

H$_2$Se.[8] However, under normal molecular-beam-epitaxy (MBE) conditions where the equilibrium vapor pressures of molecular As and Ga over GaAs are small, the steady-state composition in the near-surface region results from a balance of kinetic processes—most likely evaporation of some mixture of As, Se, and As-Se compounds from the surface (with no As$_2$Se$_3$ buildup at the sample temperature) and incorporation of Se into the surface by diffusion and As-Se exchange.

In Fig. 1, we show XPS results for a sample held at 500 °C in a 1×10^{14} (atoms/cm^2 s) Se flux for increasingly long times. Initially, the sample was in a 2×4 reconstructed, As-rich, Se-free state. (The 2×4 symmetry in fact exists over a range of surface stoichiometries so that the average surface composition of the starting clean sample cannot currently be defined from the electron diffraction alone.) The integrated peak intensities for the Ga, As, and Se 3d core levels have been converted to effective monolayers (ML's) of material.[9] The results demonstrate the evolution of the near-surface composition. The initial increase in the Se concentration corresponds closely to an immediate uptake of one effective ML. There is a concomitant and approximately equal drop in the As coverage and negligible initial change in the Ga composition. Subsequent changes occur approximately logarithmically with exposure.

The XPS and electron-diffraction results show that the first effective ML of Se is adsorbed with sticking
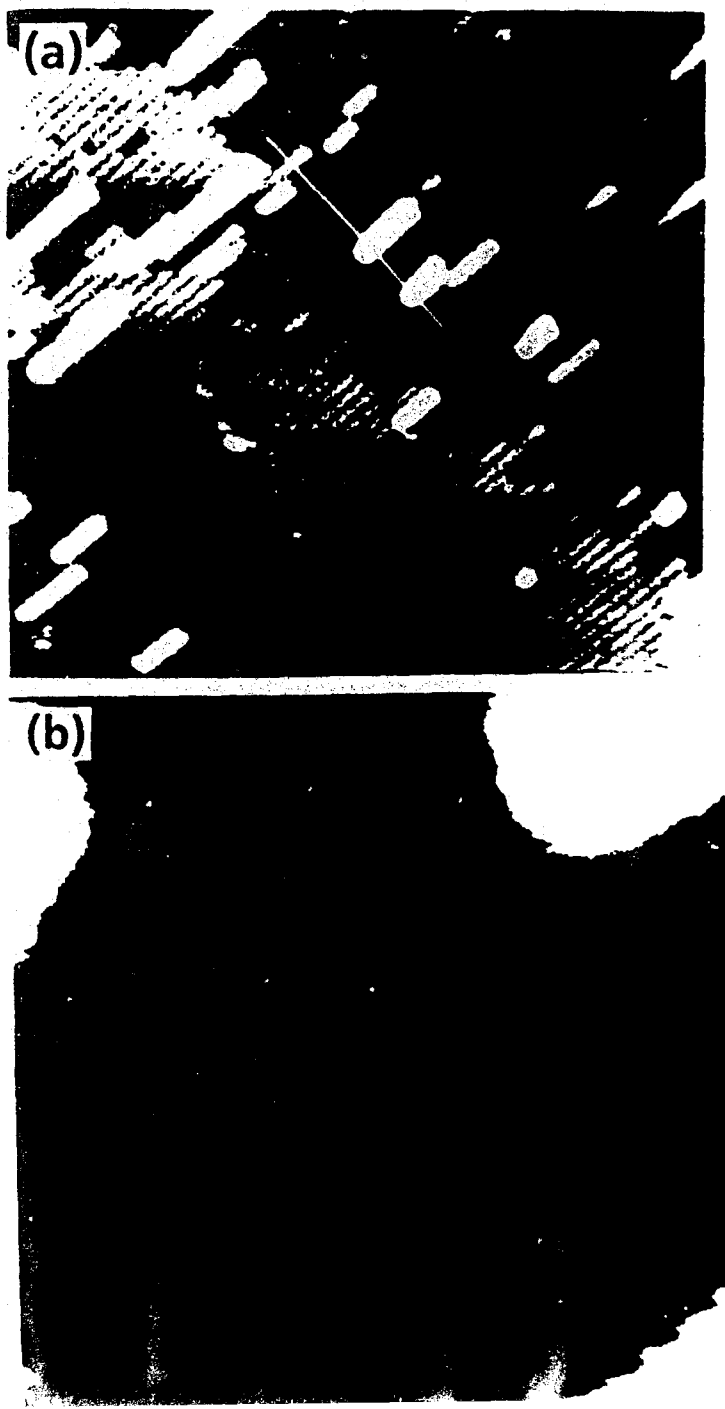

FIG. 2. STM filled state, constant current, height-keyed images of 2×1 reconstructed GaAs(100):Se 1 . . . 3.7 V, I = 50 pA. (a) 45×45 nm image with dimer rows running along the [011] direction. Diagonal white line near step edge marks trace shown in Fig. 3; (b) 5.5×5.5 nm image.
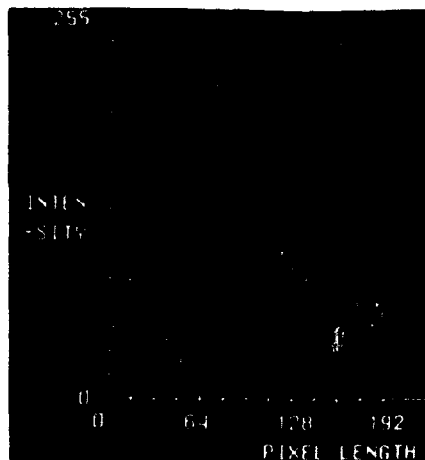
FIG. 3. Cross-sectional trace along line marked in Fig. 2(a) showing dimers, steps, and islands of one- and two-layer heights. Vertical axis full scale corresponds to 0.9 nm; horizontal axis full scale corresponds to 20 nm.

coefficient of order unity, replacing an equivalent amount of As and converting the surface into a 2×1 structure. The Se coverage then increases slowly as the As concentration drops and to a lesser extent the Ga composition drops. The formation of an epitaxial, Ga-deficient selenide (e.g., Ga_2Se_3) may thus be the limiting mechanism for Se uptake. GaSe has the same large formation energy per atom as Ga_2Se_3. However, Ga_2Se_3 is selected most likely due to its smaller lattice mismatch with the GaAs substrate.[4] Core-level shifts after Se adsorption were similar for the overlayers grown on both the Si- and Zn-doped substrates. All lines were shifted to higher binding energy by 0.2–0.3 eV (i.e., by a change in the band bending/work function) and the Ga lines, particularly the more surface-sensitive $2p$ lines, were chemically shifted still further by approximately 0.15 eV.

Surface features as revealed by STM are strikingly reproducible. Figure 2(a) is a typical filled-state image (sample bias $= -3.7$ V and tunnel current $= 50$ pA). In this case, the Se fluence was equivalent to a thickness of 4 nm. However, all images of 2×1 reconstructed surfaces have looked the same, independent of Se fluence. Rows of dimerlike features have a repeat distance of 0.8 nm just as for the dimer rows on bare GaAs(100). Figure 2(b) shows an image in which the dimers are better resolved. In contrast to bare GaAs(100), ordered arrays of missing dimers are not seen. A characteristic defect frequently observed is seen in Fig. 2(a). It is an antiphase boundary

at which a Π phase shift occurs between the equivalent dimer rows. Steps occur with a height of 0.28 nm, equal to a GaAs(100) bilayer. Long narrow islands are also a common feature. Islands are either one bilayer high (one or two dimers wide) or two bilayers high. Figure 3 shows a trace along the line indicated in Fig. 2(a). Two-bilayer-high islands are shown to be twice the height of a single-bilayer-high peninsula (which is equivalent to bilayer-high islands seen at other places in the image) as well as a step at the terrace edge. The abrupt 0.6-nm height change at two-bilayer island edges leads to strong tip convolution effects resulting both in apparently increased island width [note, for example, the broadening of the step protrusions in Fig. 2(a), which become, in effect, single-bilayer-high islands] and in increased tunneling noise induced at the island edges. Empty-state images acquired simultaneously with filled-state images show that the density of states of the dimerlike features is nearly symmetrical within the experimental noise limits. The rms noise of the dimer height measurements is approximately 0.05 Å. From traces across many dimers, an upper bound of 0.1 Å is found for the dimer asymmetry. Filled and empty states of the dimers are peaked at the same positions [similar to As-As dimers on bare GaAs(100)]. We could not achieve stable tunneling for bias voltages with magnitude less than 2.0 V.

We also studied samples similarly dosed with Te. XPS results show that, unlike the case for Se a saturated coverage of 0.5 ± 0.1 ML replaces 0.6 ML of As and leaves the Ga signal negligibly lowered. RHEED indicates a more disordered surface than the Se-covered material with strong 2×1 symmetry and weak $8 \times$ and $\times 6$ streaks often evident in agreement with previous studies.[12] Figure 4 shows a filled-state STM image, 100×40 nm^2, obtained with a sample bias of -3.9 V and a demand current of 25 pA. Long rows running again in the [011] direction with 0.8-nm spacing show a strong tendency to repel each other. The chemical identities of the constituents of the rows cannot be directly determined.

Let us first consider the results for Se-covered GaAs(100). It would be tempting to conjecture that the top monolayer consists of Se-Se dimers bonded to an ideal Ga layer below. A unit cell of such a model is shown in cross section in Fig. 5(a). In fact, this model is essentially the one proposed by Scimeca et al.[11] and Takatani, Kikawa, and Nakazawa.[7] Although the model is in reasonable agreement with the XPS results, the Se-Se dimers would result in a one-electron excess per dimer over that needed to fully occupy the bonding and lone-
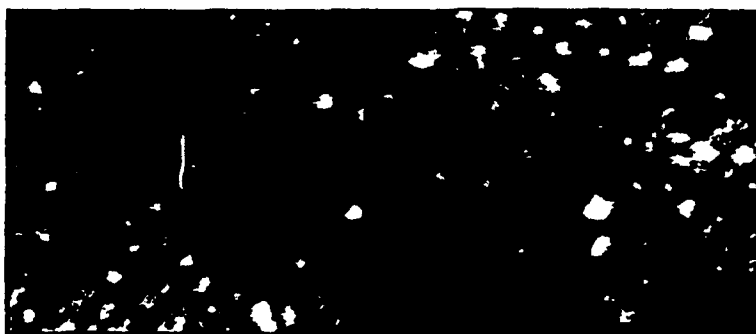

FIG. 4. STM filled state, constant current, height-keyed image of 2×1 reconstructed GaAS(100):Te ($V_{sample} = -3.9$ V, $I_t = 25$ pA). Cloudlike features are blunt-tip convolution artifacts. Again the dimer rows run along the [011] direction.
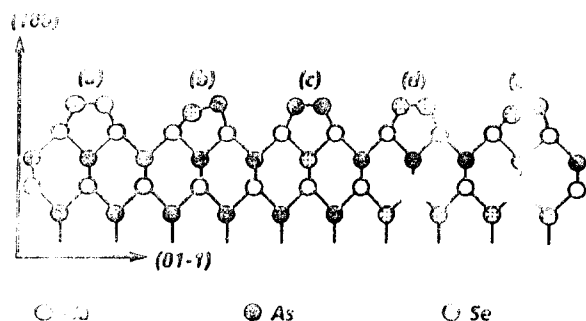
FIG. 5. Cross-sectional ball and stick models of various dimerized 2×1 cells of GaAs(100):Se.

FIG. 7. Calculated cross-sectional charge-density contours through an As-Se dimer.

pair electronic orbitals. This would be energetically very unfavorable. Based on electron counting considerations, and the tendency for Se to form twofold-coordinated structures, one might conjecture that a 2×1 Se-Se model would be unstable with respect to an autocompensated 4×1 structure with every other Se-Se dimer broken, as shown in Fig. 6. However, such a structure has not been observed. Another possible termination of the (100) surface consisting of a Se-As dimer termination is shown in Fig. 5(b). The As-Se dimers satisfy electron counting criteria. Charge transfer from the Se atom to the lone pair of the As atom would result in a closed-shell configuration for all atoms. Total-energy calculations were performed for this model using first-principles pseudopotentials and the local-density approximation.[13] The calculation predicts a Se-As dimer bond length of 2.49±0.03 Å, and a vertical separation between the Se and As atoms of 0.12±0.05 Å, with the As atom above the Se atom (i.e., nearer to the STM tip). The lone-pair orbitals of both the As and Se are filled and the As-derived states lie in a region between 0 and 1 eV below the valence-band maximum while the Se-derived lone-air resonances are 1.0–1.4 eV deeper in the valence band. Because the As lone-pair orbital are less tightly bound than those of Se, and the equilibrium position of the As atom is farther out than that of Se, the charge-density contours above the As atoms extend farther into the vacuum by 0.2 Å. This is illustrated in Fig. 7. As noted above, an upper bound on the asymmetry is estimated to be 0.1 Å. However, we still cannot rule out an asymmetric structure. Thermal vibrations of the surface atoms as well as disorder of Se-As and As-Se dimers along the dimer rows (allowing back-bond variations of the dimers) could easily lead to STM images showing
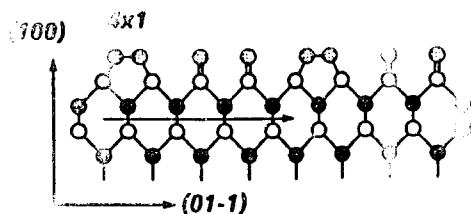

FIG. 6. Cross-sectional ball and stick model of a 4×1 cell consisting of a Se-Se dimer and two orthogonally oriented two-fold-bonded Se atoms—indicated by double lines for bonds.
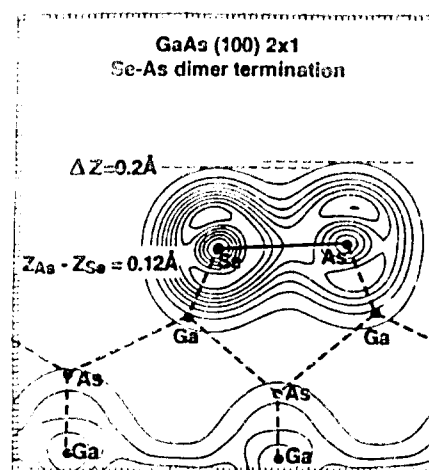
nearly symmetric features. Figure 5(c) is a model with the same composition, but with a surface Se atom exchanged with a bulk As atom. The surface dimers are symmetric and electron counting is satisfied. However, a large dipole is formed and is probably energetically less favorable.

But if the dimers are not Se-Se pairs, where then does the extra $\frac{1}{2}$ ML of Se incorporate? And what is the origin of the missing As ML? Another possibility which satisfies electron counting and does have symmetric Se-Se dimers consists of a vacancy-stabilized, reacted layer akin to Ga_2Se_3 [Fig. 5(d)]. Direct evidence in the literature for MBE creation of Ga_2Se_3 in thicker in-diffused layers has come from transmission electron diffraction on Se-reacted GaAs(100) surfaces.[5] Again, a 2×1 vacancy-related cell with lower electrostatic energy can be achieved by swapping a Se and an As vertically as shown in Fig. 5(e). The cell consists of the neutral autocompensated dimer and another autocompensated entity, the Se-terminated Ga vacancy. In principle, an arbitrary number of such vacancies could occur for mixtures of Figs. 5(a) and 5(d), or 5(b) and 5(e). For $\frac{1}{4}$ ML of Ga vacancies, we would expect to observe in XPS approximately 1 ML of Se and a reduction of the Ga by about $\frac{1}{4}$ ML and a reduction of the As by approximately $\frac{1}{4}$ ML. These numbers are arguably within the error of the XPS measurements. It is not evident, though, why a particular fractional concentration of vacancies would occur readily and then develop slowly thereafter.

The Te surface, on the other hand, fits the As-Te dimer passivation model [Fig. 5(b)] in its agreement with a $\frac{1}{2}$-ML coverage of Te. But again, what is the origin of the lost $\frac{1}{2}$ ML of As? Only a $\frac{1}{4}$-ML loss would be expected if the initial 2×4 structure of the bare GaAs consisted of the As-As dimer cells. We cannot rule out an inhomogeneous coverage consisting of unreacted areas coexisting with areas having the same structure as the Se-reacted surface.

The Pauling covalent radius[14] of As (1.17 Å) is closer to that of Se than to any of the other chalcogenides. (The

radii of S, Se, and Te are 1.04, 1.21, and 1.37 Å, respectively.) One then might expect that Se would most readily exchange with As. Furthermore, the bulk lattice constant for GaAs is 5.65 Å and those for the vacancy-stabilized zinc-blende-structured Ga_2S_3, Ga_2Se_3, and Ga_2Te_3 are listed as 5.18, 5.43, and 5.90 Å, respectively.[15] It seems likely again, therefore, that cation-exchanged material growing in epitaxial contact with GaAs would have less stress for Se than for either S or Te. It is plausible that a simple size effect is sufficient to explain the observed difference in incorporation of the different group-VI elements. The 4% lattice mismatch between Ga_2Se_3 and GaAs may nevertheless still provide a large enough stress to present a high barrier for the conversion to a nonepitaxial bulk phase at 500 °C.

We have presented an STM study of chalcogenide-terminated GaAs. The results show a well-ordered dimerized surface. The STM and XPS data alone, however, are still insufficient to solve the structure unambiguously because a multilayer composition variation exists. More deeply penetrating, near-surface-sensitive, structural probes such as medium-energy ion scattering must be applied to complement the present results.

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[2] E. Yablonovitch, B. J. Skromme, R. Bhat, J. P. Harbison, and T. J. Gmitter, Appl. Phys. Lett. 54, 555 (1989).

[3] C. J. Sandroff, M. S. Hegde, L. A. Farrow, R. Bhat, J. P. Harbison, and C. C. Chang, J. Appl. Phys. 67, 586 (1990).

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Use of ZnSe as an interlayer for GaAs growth on Si

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ZnSe has been used as an interlayer between Si substrates and GaAs layers in molecular beam epitaxial growth of GaAs on Si. It is found that thin GaAs layers are much more uniform and have fewer defects when grown on ZnSe interlayers than when they are grown directly on Si. The growth of GaAs on ZnSe is much more difficult than the more usual reverse sequence, and different growth modes for the epitaxy of GaAs on ZnSe are compared. Deposition of GaAs on ZnSe at room temperature followed by solid phase regrowth led to an epitaxial layer plus a polycrystalline layer. A slow ramping of the substrate temperature during the GaAs epitaxial growth was found to give the best crystal quality.

The major problems remaining for the successful growth of GaAs on Si are stress in the films due to differences in thermal expansion coefficients and the presence, in even the thickest films, of a high density of threading dislocations. Densities at the surface of GaAs films are typically in the range of 10^7–10^8 cm^{-2} and the lowest values which have been reproduced are around 10^6 cm^{-2}. To date, many approaches, such as temperature cycling, both during and after growth, introduction of strained layers, and special surface treatments of the substrate have been tried in order to improve this situation, but so far their effect is not sufficient to drive the dislocation density down to the 10^3 cm^{-2} range where long-lived diode lasers, for example, would be possible. In this letter we describe a molecular beam epitaxy (MBE) approach which utilizes a thin layer of ZnSe between the Si and GaAs crystals. We show that very uniform films with a combined thickness of 50 nm can be grown, and we will also describe a new method for growing GaAs on ZnSe.

The use of a ZnSe interlayer has two advantages over direct growth of GaAs on Si. ZnSe was first proposed[1-3] as an interlayer between GaAs and Si because it is softer than either GaAs or Si (the Knoop hardness for Si, GaAs, and ZnSe is 1150, 750 and 150, respectively). This suggests that it is possible that dislocations can be forced to reside in the interlayer instead of propagating into the GaAs film, and that dislocations in the GaAs can be squeezed out into the ZnSe layer by thermal cycling sequences. The second advantage is that ZnSe films of very uniform thickness can be grown on Si at thicknesses where GaAs films grown directly on Si are dominated by island formation and coalescence.[2,3] The ZnSe therefore serves initially as a good template for GaAs growth (the lattice constants and thermal expansion coefficients of GaAs and ZnSe are comparable when compared with their differences from those of Si) and then after the GaAs is grown the ZnSe may serve as a sink for dislocations.

The use of a thick (0.5 μm) ZnSe film as in interlayer in metalorganic chemical vapor deposition growth of GaAs on Si has been described recently[4] and the authors of that study found that the resulting GaAs was of better quality than control samples in which no ZnSe layer was present. In this letter we take a more fundamental approach and

examine the growth modes of very thin layers. The use of thin layers has the advantage that a dislocation net can be kept very close to the substrate. Minimization of the amount of ZnSe required also means that use of a ZnSe compound source in a MBE system dedicated to GaAs is workable. We will show that very uniform films of ZnSe and GaAs with a combined thickness of around 50 nm can be grown on Si. The MBE growth of uniform ZnSe layers on Si has been discussed in detail elsewhere[2,3] and will only be briefly described here. We will concentrate instead on the technique required to achieve epitaxial growth of GaAs onto these ZnSe-on-Si layers.

GaAs growth on ZnSe is considerably more difficult than the much-studied inverse growth of ZnSe on GaAs because the optimum temperature for GaAs growth ($\sim$600 °C) is high compared with that ($\sim$300 °C) used for ZnSe MBE. Nevertheless, successful growth of GaAs on high quality ZnSe layers (epitaxially grown on GaAs substrates) has been achieved recently.[5,6] Tamargo et al.,[5] found that the surfaces of GaAs grown on ZnSe at 300 °C were initially rough and that the final GaAs layer contained a large number of microtwins. They attributed this to the fact that As bonding to the final Zn layer of the ZnSe leads to electron-deficient Zn—As bonds. It was subsequently proposed[7] that growth onto the ZnSe(100) $c(2 \times 2)$ surface (which has 1/2 ML of Zn as its outermost layer) would be optimized by adding 1/2 ML of Ga to that surface before exposure to As. This would yield equal numbers of Ga—Se and Zn—As bonds and neutralize the interface. Kobayashi and Horikoshi[7] were able to achieve good GaAs epitaxy on ZnSe by using a combination of solid phase epitaxy (SPE) and migration enhanced epitaxy, the alternate supply of group III and group V species to the growth surface. Their best GaAs films were obtained by initiating the growth on ZnSe with an As$_4$ exposure at room temperature (RT) followed by deposition of two Ga monolayers at RT.

In the case of ZnSe as an interlayer between Si and GaAs, we wish to keep the ZnSe layer on Si as thin as possible and, therefore, the growth of GaAs must occur on a surface that is not yet completely smooth. We will describe a growth method which does allow GaAs to be grown successfully on ZnSe in this situation. We have also
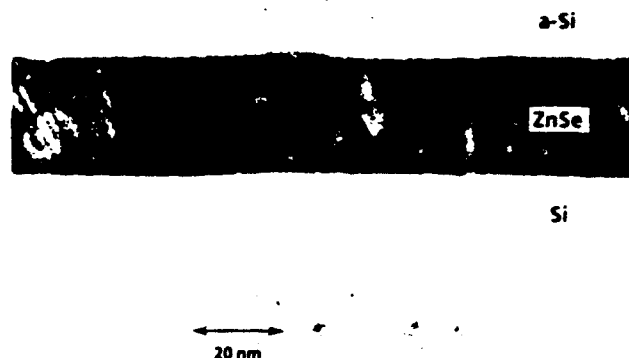
FIG. 1. TEM cross section, in the [011] projection, of a ZnSe film deposited on arsenic-terminated Si(100) at 300 °C. All TEM samples were coated with a film of amorphous Si prior to thinning.
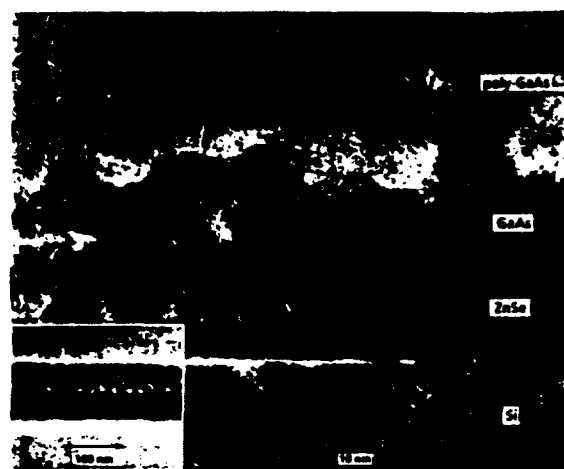

FIG. 2. Cross-sectional TEM lattice image in the [011] projection, of a GaAs film grown on ZnSe-coated Si. A lower resolution image of the same region is shown in the insert. The ZnSe film is epitaxial with respect to the Si substrate and was prepared in the same manner as the ZnSe film in Fig. 1. The first 8–10 nm of the GaAs film is epitaxial with respect to the ZnSe and the remainder appears to be polycrystalline GaAs. The GaAs film was deposited at RT and annealed to a maximum temperature of 500 °C.

found an interesting aspect of the epitaxial process which has general applicability to other epitaxial processes.

The silicon substrates used were oriented so that their surface normals were 4° from the [100] direction, with the tilt being towards one of the ⟨011⟩ directions. Clean surfaces were prepared and then passivated with a monolayer of As prior to the deposition of 10–50 nm ZnSe films.[3] The As monolayer allows the ZnSe to grow on Si at elevated temperatures without a reaction taking place between the Si and Se atoms[3] and leads to charge balance at the interface.[8] The GaAs and ZnSe were grown using effusion cells containing Ga, As, and ZnSe in an ion- and cryo-pumped chamber with liquid-nitrogen cold shrouds to maintain a clean ambient.

Growth of ZnSe on Si(100): As at substrate temperatures in the range 250–300 °C gave rise to films with uniform thickness and with relatively smooth surfaces.[3] The transmission electron microscope (TEM) image of such a film in Fig. 1 should be contrasted with the equivalent situation for GaAs on Si where island formation and coalescence dominate for thicknesses below about 100 nm.[9] [We note that the GaAs growth on Si(100) also begins on an As-terminated surface, but the same electron counting arguments that favor an interface region with a stacking sequence of atomic planes of -Si-Si-As-Zn-Se-Zn- show that -Si-Si-As-Ga-As- is energetically unfavorable.]

Several growth methods were investigated in order to compare the quality of GaAs grown on these ZnSe-on-Si layers. The initiation stage was found to be the most crucial, in agreement with the previous studies[5,6] of GaAs on ZnSe. One of our main goals is to find a method that does not require (i) the complication of using a migration enhanced epitaxy technique or (ii) having a particular ZnSe surface reconstruction. As a result, we have used straightforward MBE techniques but modified them at the beginning of the growth. The most successful method utilized a slow ramping of the temperature during the MBE growth of the GaAs.

GaAs growth cannot be initiated on ZnSe at substrate temperatures around 600 °C, which are typical for GaAs

homoepitaxy. When GaAs was nucleated on ZnSe at temperatures above 300 °C we found that the GaAs films grew via island formation and coalescence. Deposition of GaAs at RT followed by SPE, on the other hand, yielded epitaxial GaAs close to the interface and the remainder of the GaAs film was found to be polycrystalline. This is similar to the behavior seen in SPE of amorphous Si, where the distance of successful epitaxial propagation away from a single crystal substrate depends on the rate of SPE relative to the rate of random crystallization in the amorphous part of the film.[10] This competition leads to a maximum epitaxial thickness for a given set of conditions. In our situation, the thickness of the GaAs that was epitaxial was found to be very sensitive to the annealing sequence and was rather irreproducible. A cross-section TEM image of a GaAs film that was deposited at RT on the ZnSe interlayer and then annealed with a slowly increasing temperature ramp up to a maximum temperature of 500 °C is shown in Fig. 2. The epitaxial region near the GaAs/ZnSe interface in this case has an average thickness of about 8 nm out of a total GaAs film thickness of around 50 nm. The interface between epitaxial GaAs and the polycrystalline GaAs is undulating and exposes atomic planes, e.g., {111}, which make large angles with the (100) growth plane. The same behavior is seen in all of the GaAs films which were grown on ZnSe via RT deposition and SPE. This indicates that the best approach for growth using SPE is to nucleate a very thin film of GaAs, anneal it to form an epitaxial layer, and then grow GaAs "homoepitaxially" on this GaAs template. Use of the thinnest possible layers is also found to give the best quality films by RT deposition and SPE of GaAs grown directly on Si.[11]

A similarly shaped boundary between epitaxial and amorphous material has been seen by Eaglesham et al. in the low-temperature homoepitaxial growth of Si on
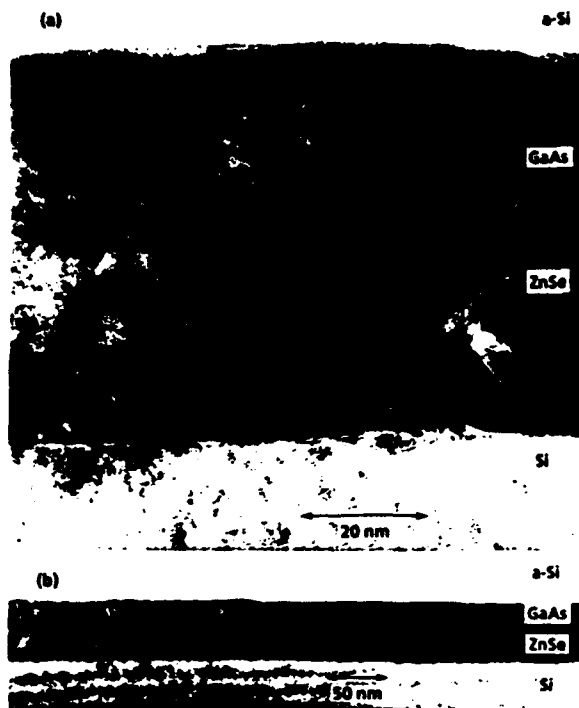
FIG. 3. TEM cross section at (a) higher and (b) lower resolution, in the [011] projection, of a GaAs film grown on ZnSe-coated Si. Both the ZnSe and GaAs films are epitaxial with respect to the Si substrate. During deposition of the GaAs film, the substrate temperature was raised from 150 to 500 °C.

The TEM image shows that the GaAs film is epitaxial with respect to the ZnSe interlayer and to the Si substrate. It has a relatively uniform thickness with good surface morphology, in contrast to the results typically obtained when GaAs is grown directly on Si. There is no evidence of growth via island formation and coalescence, and the interface between the ZnSe and the GaAs is rather featureless. The major defects present in the ZnSe interlayer are microtwins and some of these terminate at the ZnSe-GaAs interface and others propagate into the GaAs film. It has been shown[14] that postgrowth annealing is effective in removing microtwins from GaAs on Si and we expect that the same will apply here.

In conclusion, we have shown that GaAs films grown on Si with an intermediate layer of ZnSe have a significantly better morphology in the 0–100-nm-thickness regime than do GaAs films grown directly on Si. Work to grow thicker GaAs films onto these templates is currently underway so that the threading dislocation density can be characterized and the effects of postgrowth annealing investigated.

We have also found that by slowly ramping the substrate temperature, it is possible to increase the epitaxial thickness for III-V materials which are initially deposited at low temperatures.

Si(100)[12] and GaAs on GaAs(100).[13] They found that epitaxial growth would occur at low temperatures until a critical thickness at which surface roughening led to a transition to amorphous growth. This suggested that the thickness of the epitaxial film that could be grown could be increased by growing at reduced substrate temperatures, interrupting the growth, annealing, and then resuming the growth at the lower substrate temperature.

We have found that a modification of this technique allows us to obtain uniform, epitaxial GaAs films on ZnSe interlayers. By slowly ramping the temperature during growth we have avoided the requirement to interrupt the growth. This reduces both the growth time and the degree of contamination as well as simplifying the overall technique. The TEM image in Fig. 3 is from a GaAs film that was deposited at temperatures between 150 and 500 °C. Specifically, after the ZnSe film was grown at 300 °C on Si(100): As, the substrate was held at 300 °C while the As and Ga sources were warmed up, then the substrate temperature was dropped to 150 °C. The GaAs was grown for 3 min at each of the temperatures in the sequence: 150, 200, 250, 300, 350, 400, 450, and 500 °C.

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THREADING DISLOCATION DENSITIES IN GaAs GROWN ON REDUCED AREA Si SUBSTRATES

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ABSTRACT

We have studied the possibilities of reducing the threading dislocation (TD) density in GaAs on Si using free side wall growth on patterned Si substrates and/or using a soft ZnSe interlayer in combination with post growth annealing procedures. TD densities were accurately determined using large area plan view TEM and were found to be unaffected by proximity to free side walls and by the ZnSe interlayer. Post growth heat treatments led to a factor of ~2 reduction in TD density and to bunching of dislocations throughout the thickness of the film.

INTRODUCTION

GaAs on Si technology is still limited by a high density of threading dislocations (TDs), which is attributed to the 4% lattice mismatch and the large difference in thermal expansion between GaAs and Si. The lattice mismatch introduces a high density of misfit dislocations which can terminate either at the film surface or at the sample edge. Fitzgerald found that for systems with smaller lattice mismatch (<0.4%) TD densities can be reduced by reduction of the growth area [1]. In addition, post growth patterning and annealing has been observed to reduce the density of dark line defects in GaAs on Si [2]. Sohn et al [3] grew GaAs on Si mesas and observed a slight reduction in etch pit density with reduced mesa size. However, the mesas in that experiment did not provide free sidewall growth. In this paper we report on a study of the growth of GaAs on Si where free side walls exist during deposition. The effects of a soft ZnSe interlayer and post growth annealing procedures are also described. TDs were observed directly by large area plan view transmission electron microscopy (TEM).

EXPERIMENTAL DETAILS

GaAs films on Si were grown by conventional two step MBE to a thickness of ~2 μm (growth temperatures 400° C and 600° C). ZnSe layers were deposited at a substrate temperature of 300° C on an As terminated Si surface from a compound source in the same growth chamber. A detaild description of the procedures used for growth of GaAs on ZnSe and of ZnSe on Si is given in reference [4].The Si substrates were misoriented 4° off from the [001] towards [110]. The substrates were patterned with square mesas with dimensions ranging from 5 to 35 μm. To make the films grow with free side walls the mesas were fabricated to have overhanging side walls using a technique shown in Fig. 1. Post growth anneals consisted of either (i) a slow anneal to 850° C for 15 min followed by a slow 3 hour cool down to room temperature, or (ii) a rapid thermal anneal (RTA) to 800° C for 30 sec which was repeated 5 times. The slow anneal was performed in sealed and evacuated quartz tubes with As enclosed. During RTA the sample was sandwiched between GaAs wafers in flowing N_2 gas. Accurate determination of defect densities using TEM was made possible by a novel sample preparation technique (see Fig. 2). The samples were mechanically thinned from the back side followed by plasma etching in CF_4. The CF_4 etch selectively removed Si leaving a free standing GaAs film with an area of ~1mm². This film was subsequently thinned to electron transparency by ion milling. To maintain the mechanical stability of a large thin TEM foil and to prevent mesas from falling out a polyimide (PI) layer was deposited on the film side prior to the mechanical thinning. This layer was later partially etched away leaving a supporting PI grid.
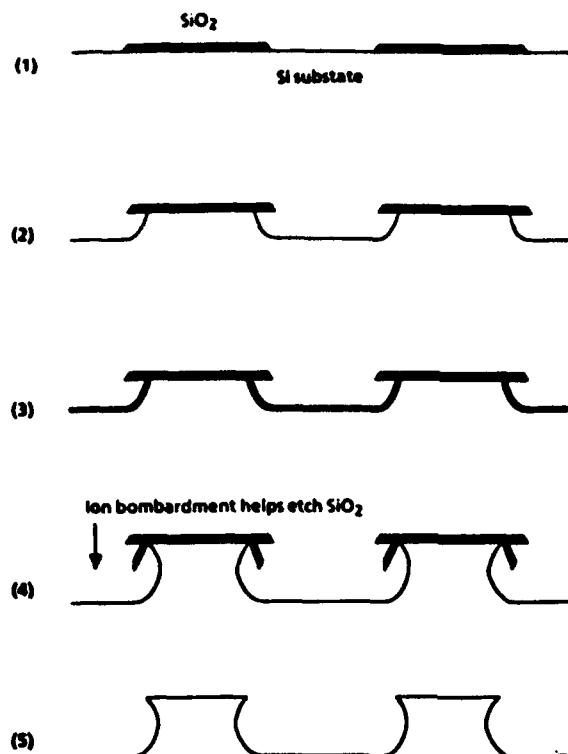
Figure 1. Si mesa fabrication: (1) Grow a 350 nm thermal oxide on a Si wafer and pattern it with photolithography. (2) Plasma etch with CF_4. (3) Grow 50 nm thermal oxide in vias. (4) Plasma etch with CF_4. The overhanging oxide slows down the etching of the oxide on the via side walls. The side wall oxide will be undercut due to the much higher etch rate for Si. (5) Remove oxide with HF.
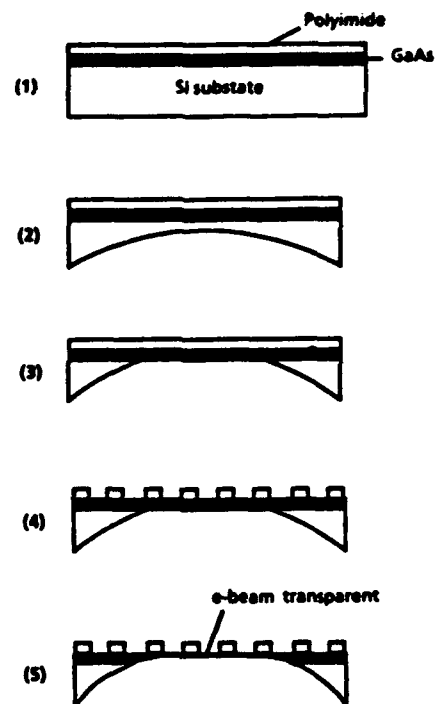
Figure 2. TEM sample preparation: (1) Spin polyimide (PI) on sample. (2) Cut 3mm disc and dimple from substrate side. (3) Plasma etch with CF_4 from substrate side. (4) Partially remove PI using O_2 plasma etch and a masking grid. (5) Ion mill from substrate side.

RESULTS

Figure 3. shows plan-view TEM images from the top 200 nm of a 2 μm GaAs film grown on Si mesas having 20 μm sides ((a) as grown and (b) after an anneal to 850° C for 15 min). A number of such large area plan views were analyzed providing TD densities that were accurate to within 50 %. No significant difference in TD density was found when comparing layers grown on mesas (with dimensions of 5 to 35 μm) with films on continuous substrates. Table I summarizes the dislocation densities for as grown layers, layers after a slow anneal and after RTA. Data for GaAs grown directly on Si and on a ZnSe interlayer is given together with the densities for a pure 2 μm ZnSe film grown on Si. In the data for as grown material we observe a TD density of approximately 6×10^8 cm^{-2} for GaAs both with and without the ZnSe interlayer. We also see a similar density for the pure ZnSe layer. After both slow
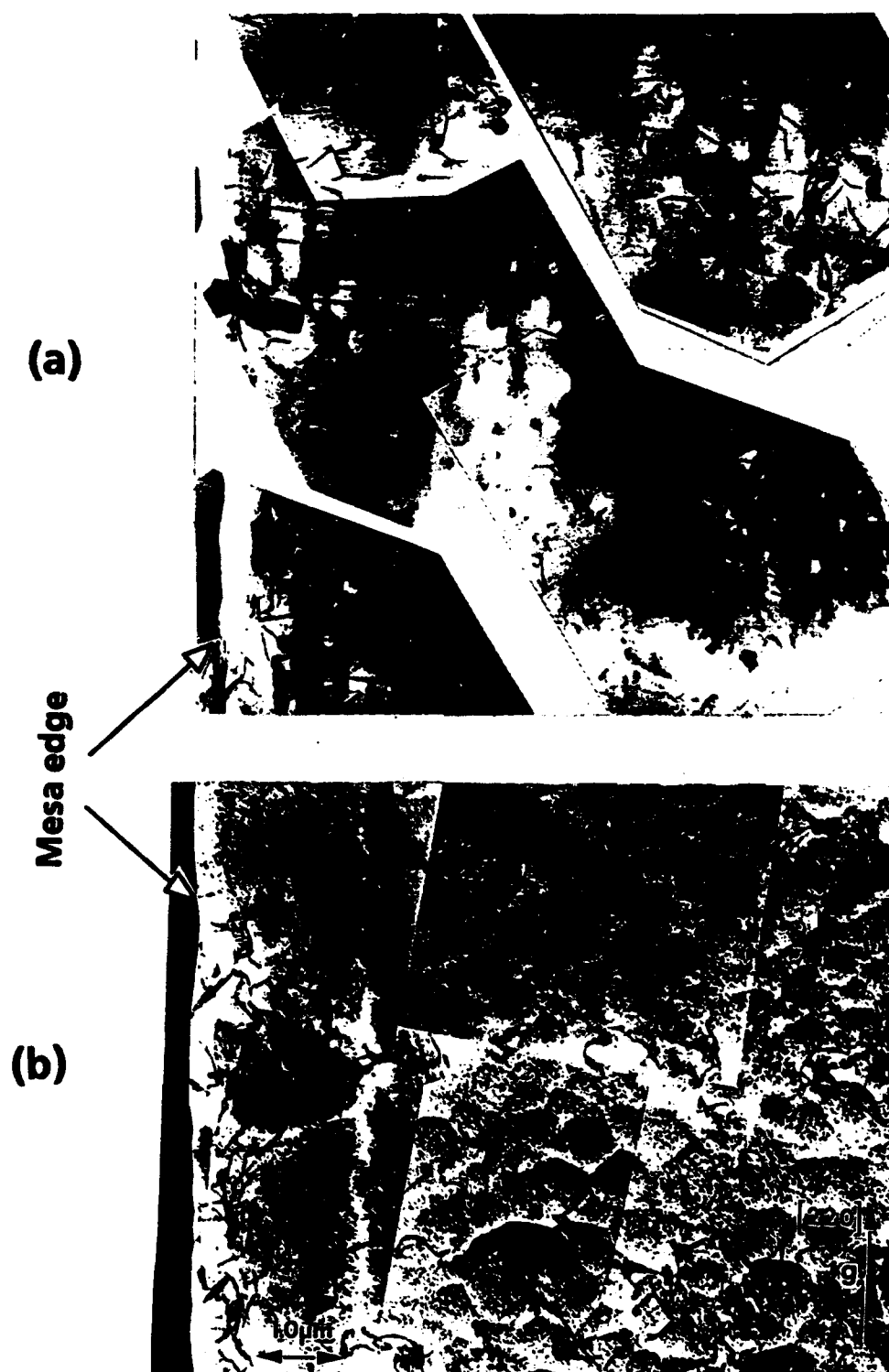
Figure 3. TEM plan view micrographs of GaAs film on 20 μm Si mesas (The diffraction vector was the [220] near the [001] zone.). (a) As grown, (b) after anneal to 850° C for 15 min followed by a slow cool down to room temperature over 3 hours.

Table 1. Threading dislocation densities

	GaAs on Si $[10^8\,cm^{-2}]$	GaAs on ZnSe on Si $[10^8\,cm^{-2}]$	ZnSe on Si $[10^8\,cm^{-2}]$
As grown	6	6	7
RTA, 800° C, 30 s 5 times	7	6	5 (RTA to 550° C)
850° C, 15 min with slow cool	3	4	

anneal and RTA a small reduction in TD density is detected. Another effect of post-growth heat treatment can be seen by comparing Fig. 3(a) and 3(b). After anneal, a majority of the dislocations appear entangled whereas in the as grown film most of the dislocations are unentangled throughout the top part of the film. The bunching must be the result of dislocation reactions that occur as dislocations become mobile at high temperature and/or when new dislocations are introduced during the annealing and cool down.

Burgers vector analysis using the $g.b = 0$ criterion and stereo imaging was used to determine the structure of the dislocations. Figure 4 shows TEM micrographs of an as grown film. TDs marked with a and b have Burgers vectors of $<110>$ type that make an angle of 45° with the surface plane and TDs marked with c_1 and c_2 have Burgers vectors of $<110>$ type lying in the surface plane. We observed that both in annealed and unannealed films, only $\sim 20\%$ of the dislocations have a Burgers vector parallel to the surface plane. From our stereo images it was found that unentangled dislocations often had line directions either along $<110>$ or $<112>$ directions. Close to mesa edges many dislocations were found to follow the $<112>$ direction that pointed away from the edge when going from substrate to film surface. This could be related to the asymmetric stress that prevails near the edges.

The dislocation density is much higher close to the substrate than at the surface of a 2 µm film as can be seen in the TEM cross section of an as grown film in Fig. 5. This is due to a large number of dislocation reactions between threading segments that leads to annihilation and /or superposition of threading segments.

DISCUSSION

The result that proximity to free side walls does not strongly affect the TD density can be interpreted in two ways. Either (i) the films are dislocation free at high temperature and TDs move in during cool down because of thermal expansion mismatch or (ii) the threading segments are always present and have low mobility due to interactions at the interface. The fact that the threading dislocations were unentangled throughout the top part of the unannealed films indicates that these dislocations have not moved far during cool down from the growth temperature. This leads us to suggest that they are present already during growth. It is probable
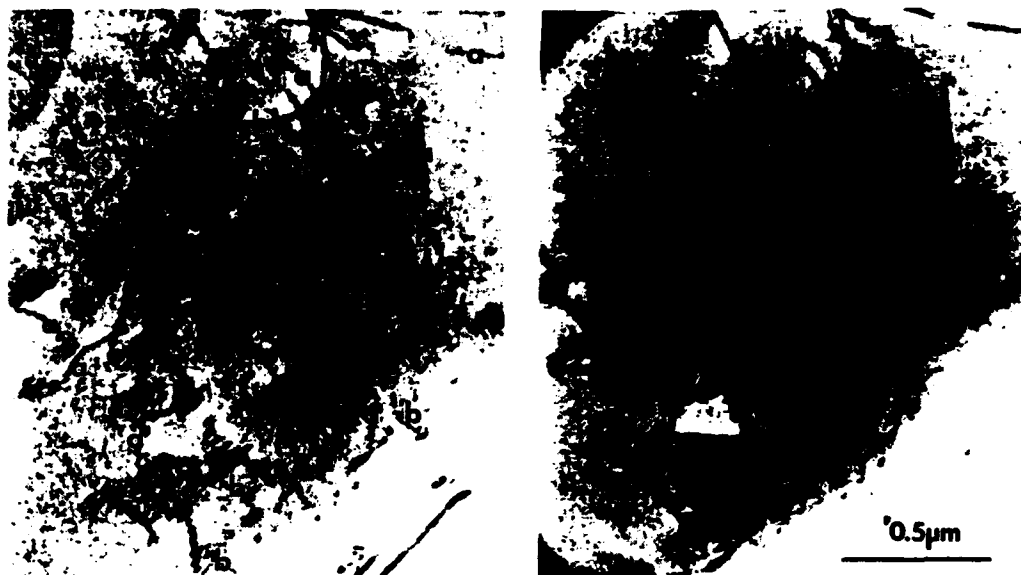
Figure 4. TEM plan view of an as grown GaAs film on a 10 µm Si mesa (near a [001] zone). In the left panel the diffraction vector g was [220], and in the right g was [040]. In the micrographs the label "a" indicates dislocations with Burgers vector $b = \pm \frac{1}{2}a[110]$ or $b = \pm \frac{1}{2}a[1\bar{1}0]$, the label "b" indicates $b = \pm \frac{1}{2}a[101]$ or $b = \pm \frac{1}{2}a[10\bar{1}]$, "$c_1$" indicates $b = \pm \frac{1}{2}a[110]$, and "$c_2$" indicates $b = \pm \frac{1}{2}a[1\bar{1}0]$.

Figure 5. TEM cross section of as grown GaAs film on 10 µm Si mesa. The foil normal was [110] and the diffraction vector was [220].

that these dislocations are the result of interactions between many threading segments leaving the substrate interface and reacting to form a single threading segment that continues to the surface. The protruding dislocations will have a greatly reduced mobility due to their entangled "roots" and we refer to them as slow TDs. During growth most of the dislocation reactions take place at an early stage while the dislocation density is high and the dislocations move to gradually relax the strain caused by lattice mismatch. This gives the well known high defect density throughout the first 0.5 μm of the film (see Fig. 5). During subsequent growth the film is relaxed and the density of threading segments is low leading to a substantial reduction in the probability of dislocation reactions. During cool down to room temperature the system strives to remove a fraction of the misfit dislocations at the interface to partially accommodate the thermal expansion mismatch between GaAs and Si. A misfit segment of 60° type can be eliminated through glide to the surface. This process only removes a component from each of two slow TDs and will in general only change the Burgers vector of the slow TDs but not eliminate them. When the sample is reheated after growth new misfit segments will form through nucleation and multiplication. The corresponding threading segments will move and interact with new and old TDs at all levels of the film. This is consistent with the observation of numerous entangled TDs in the top layer of a post growth annealed film.

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Threading dislocations in GaAs grown with free sidewalls on Si mesas

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Abstract

We have studied the mechanisms that determine the density and structure of threading dislocations (TDs) in GaAs on Si by growing GaAs films on continuous Si substrates and on 10-34 µm wide Si mesas that provided free sidewall growth. The effects of a soft ZnSe interlayer and of post growth annealing to 850° C were also investigated. TD densities were accurately determined using large area plan view transmission electron microscopy (TEM). Burgers vector analysis of the TDs showed that threading segments associated with both sessile 90° misfit dislocations and glissile 60° misfit dislocations were present after growth. A difference in dislocation structure between the annealed and unannealed samples was observed. It was also found that the dislocations were unaffected by proximity to free sidewalls and by the ZnSe interlayer. The results indicate that dislocation interactions during the early stages of growth determine the structure and density of TDs in as-grown films. It was also concluded that plastic relaxation of thermal mismatch strain during cool down from the growth temperature does not strongly affect the TD density in the films. This is in contradiction to previous studies.

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I . INTRODUCTION

The continued interest in GaAs growth on Si is stimulated by the high potential for technological applications of the integration of an optoelectronic material with Si. High threading dislocation (TD) densities have been a barrier to the success of this heteroepitaxial system. Several techniques for reduction of threading dislocation densities have been identified and tested[1-3], but none so far has reduced the density to levels that enable long-lived laser diode operation. To effectively pursue the goal of low threading dislocation densities for GaAs grown on Si, further work is needed to increase the understanding of the mechanisms that lead to the high TD densities that are presently observed.

Threading dislocations are associated with misfit dislocations (MDs) at the interface which are necessary to accommodate the lattice mismatch between Si and GaAs. The MDs can terminate either at the film surface via threading dislocations or at a film edge. For good quality TD-free GaAs the desired state is obtained when all MDs terminate at the edge of a film. Two types of MDs are present at the interface: 90° (Lomer) dislocations, which are sessile and have a Burgers vector **b** that lies in the interface plane, and 60° dislocations, which are glissile and have **b** out of the interface plane. A 60° MD can change its length during plastic relaxation by glide of the corresponding threading segments whereas a 90° MD can only change its length by climb of its associated TDs. Glide is a much faster process than diffusion-limited climb and we expect glide to be the dominant mechanism for plastic deformation in the presence of threading segments associated with both sessile and glissile MDs. As a clarifying remark it should be pointed out that the notation sessile and glissile does not refer here to the threading segments but merely to the misfit segment of a dislocation. The fact that only the threading segments that are associated with 60° misfit dislocations can contribute to plastic relaxation of misfit stress by glide motion is due to the in plane orientation of the misfit stress[4].

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GaAs and Si have a 4.02 % lattice mismatch at room temperature which changes to 4.19 % at a typical growth temperature of 600 °C due to a large difference in thermal expansion coefficients. The role of this thermal expansion mismatch in the formation of TDs is not completely understood. A previous investigation by Tachikawa and Mori suggested that in the case of VPE growth of GaAs on Si most of the TDs were introduced during cool down by the thermal mismatch strain[5]. However, this mechanism does not explain the high TD densities observed, for example, for growth of InGaAs on GaAs at comparable lattice mismatch to the GaAs/Si system but much smaller thermal expansion mismatch[6].

In this paper we present a study of the growth of GaAs on Si mesas which were designed to provide free sidewalls during growth. The availability of free sidewalls is intended to make it easier for MDs to terminate at film edges rather than by threading. The results provide insight to the mechanisms of relaxation during cool down after growth and have enabled us to rule out thermal mismatch as a major contributor to the TD density. We have also studied the possibility of enhancing the mobility of TDs by interposing between the GaAs and Si a layer which has a much higher dislocation mobility than GaAs. We used ZnSe which has a hardness that is only 20% of that of GaAs and is relatively well lattice-matched to GaAs (~ 0.3% mismatch). In addition TD densities for GaAs films on Ge were obtained for comparison.

II. EXPERIMENT

GaAs and ZnSe films as well as structures consisting of GaAs on a 0.25 μm thick ZnSe interlayer were grown on patterned and continuous Si substrates. GaAs films were also grown on continuous Ge substrates. The total film thickness was typically ~2 μm. The substrates were cut so that their surface normals were oriented 4° from [001] towards the [1$\bar{1}$0] direction. To obtain free sidewall growth on Si by MBE we fabricated mesas with overhanging sidewalls. This was achieved with a two step

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oxidation and plasma etch process (see fig. 1). A 350 nm thick thermal oxide was grown on the substrates and patterned using a photoresist mask and etching with HF. The exposed Si was then etched in a $CF_4 + O_2$ plasma which etches the oxide a factor of 10 more slowly than the Si. The sample was again thermally oxidized providing a 70 nm oxide in the vias. Plasma etching of SiO_2 is strongly dependent on ion bombardment from the plasma. Therefore, when the sample was again subjected to the $CF_4 + O_2$ plasma the thin oxide at the bottom of the vias was etched. However, the oxide on the sidewalls was not etched because it was protected from ion bombardment by the under cut top oxide. The exposed Si at the bottom of the vias was then etched isotropically and undercutting of the side wall oxide produced the desired profile. The mesa mask that was used produced mesas with widths ranging from 10 to 35 µm.

The GaAs films on Si and Ge were grown by conventional two step MBE (typically 0.1 µm grown at 400 °C and subsequent growth at 600 °C). ZnSe layers were deposited at a substrate temperature of 300 °C on an arsenic-terminated Si surface using a ZnSe compound source in the same growth chamber. Detailed descriptions of the procedures used for growth of GaAs on ZnSe and of ZnSe on Si have been published previously[7]. After growth, specimens taken from wafers were annealed to 850 °C for 15 min. followed by a slow 3 hour cool down to room temperature. The anneal was performed in sealed and evacuated quartz tubes with solid As enclosed. (The As_4 pressure was ~2 Atm. during the anneal).

Accurate determination of defect densities using TEM on plan view samples was made possible by a novel sample preparation technique (see Fig. 2). A polyimide layer was first deposited on the film side to maintain the mechanical stability of a large thin TEM foil and to prevent mesas from falling out when the substrate was removed. This layer was later partially removed by O_2 plasma etch to planarize the sample and to leave the top of the mesas free of polyimide. The sample was then

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mechanically thinned and dimpled from the back side followed by plasma etching in CF$_4$. The CF$_4$ etch selectively removed Si leaving a free standing film of continuous GaAs or polyimide supported GaAs mesas with an area of ~1mm^2. This film was subsequently thinned to electron transparency (0.3-0.4 μm) by backside ion milling. The specimens were examined in a JEOL 4000 TEM operated at 300 kV. Burgers vector analysis on plan view samples was obtained with two-beam images near the [001] zone (Only the [001] zone was used due to limited tilt capabilities in the microscope.). Diffraction vectors g = (040), (400), (220) and ($\bar{2}$20) were used.

The perpendicular lattice parameters of the films were measured using x-ray diffraction and the in-plane lattice parameter was calculated from the perpendicular using elastic constants of the film material[8].

III. RESULTS AND DISCUSSION

Our main objective is to examine the dynamics of TD (threading dislocation) formation and the effects of reduced area growth for a heteroepitaxial system with a large lattice mismatch and a large thermal expansion mismatch. However, to set a baseline, and to make sure that most of the TDs that we are observing are related to the mismatch of the system, we begin with a brief discussion of GaAs on Ge where the mismatches in lattice parameter and thermal expansion are small, and then show the different behavior that occurs for GaAs and ZnSe on Si.

A. GaAs on Ge

Figure 3 shows a plan-view TEM image from a 2 μm thick GaAs film grown on a continuous Ge substrate. The TEM specimen consists of the top ~400 nm of the film. Only two TDs appear in the image which covers an area of ~200 μm^2. (One of the dislocations has a Burgers vector such that g·b=0 and shows very weak contrast.) The average TD density (ρ_{TD}) for this type of sample was estimated to be 5($\pm$4)x10^5

cm^{-2} by measuring an area containing 8 dislocations in the microscope. Three stacking faults were also observed in the same area. This TD density is three orders of magnitude lower than that typically observed for GaAs on Si and is close to being acceptable for minority carrier device application.

B. GaAs on Si

A plan-view TEM image from a 2 µm thick GaAs film grown on a Si mesa with 24 µm width is shown in Fig. 4a. The average TD density (ρ_{TD}) for this type of sample is 7 ($\pm$3)x10^8 cm^{-2}. Values of ρ_{TD} were also obtained from films grown on mesas of different sizes as well as on continuous substrates. We found that the density does not, in fact, depend on the growth area in the range studied here. The TDs are mostly isolated and unentangled throughout the TEM foil. A plan-view of a similar 2 µm thick GaAs film on a 24 µm mesa which has been annealed to 850° C for 15 min after growth is shown in Fig. 4b. The TD density is 4x10^8 cm^{-2} which is slightly lower than for the unannealed film and again was found to be independent of substrate growth area. The major difference in dislocation structure between the as-grown and the annealed film is that in the annealed film the dislocations have interacted and are entangled throughout the top layer of the film whereas the TDs are free and unentangled in the as-grown film.

The Burgers vectors of dislocations can often be determined by obtaining several two-beam diffraction contrast images of the same dislocations with different diffraction vectors, $\mathbf{g}$, active. A dislocation with $\mathbf{b}$ such that $\mathbf{g} \cdot \mathbf{b} = 0$ will show reduced contrast and will be completely invisible if also $\mathbf{g} \cdot \mathbf{b} \times \mathbf{u} = 0$, where $\mathbf{u}$ is a unit vector in the direction of the dislocation line. We have recorded images in two-beam conditions using the diffraction vectors $\mathbf{g}$ = (040), (400), (220) and ($\bar{2}$20). Since glissile MDs have $\mathbf{b}$ along (011), (0$\bar{1}$1), (101) or ($\bar{1}$01) and sessile MDs have $\mathbf{b}$ parallel to (110) or ($\bar{1}$10) this allows us to distinguish between TDs that are associated with sessile and

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glissile MDs. From analysis of the Burgers vectors of the dislocations we found that TDs associated with glissile and sessile misfit dislocations were present in both as-grown and annealed samples. Approximately 60% of the dislocations were associated with glissile MDs (**b** out of the interface plane) and 20% with sessile MDs (**b** in the interface plane.) The remaining 20% of the dislocations could not be unambiguously determined due to limitations in the tilt available in the microscope. An example of images used for **b** determination is shown in Fig. 5 for an as-grown GaAs film on a 10 μm Si mesa. Only two of the four diffraction conditions taken from the same area in the GaAs film are shown. TDs associated with glissile and sessile MDs are indicated by the letters "G" and "S", respectively.

These observations have led us to conclude that a large fraction of the TDs that are observed in the samples after growth and cool down must also have been present during growth. As mentioned in section I, due to the very low mobility of TD associated with sessile MDs, only the TDs associated with glissile MDs are expected to move in response to a misfit strain induced during cool down by thermal expansion mismatch. The density of TDs associated with sessile MDs, which was measured to be $\sim 1 \times 10^8$ cm^{-2} at room temperature, is thus expected to have been the same before cool down. Furthermore, the observation of mainly unentangled dislocations in the as grown films indicates that they have not interacted during cool down. Otherwise they would have bunched together in the same way as in the annealed films. Using a simple estimate of interaction cross sections this shows that even the TDs associated with glissile MDs can only have moved a short distance of ≤ 3 μm during cool down. This implies that these TDs also were present during growth.

We have performed x-ray diffraction (XRD) measurements of the lattice parameter of the GaAs film on continuous substrates. If we assume that the GaAs is completely relaxed at the growth temperature and that no dislocation motion (plastic deformation) occurs during cool down we would expect approximately a 0.2

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% biaxial tensile strain in the as-grown layer. The x-ray measurements show that the films exhibit a 0.1% in-plane tensile strain. This is due to a combination of the thermal expansion mismatch stress and a partial plastic relaxation of this stress. This means that the plastic relaxation to relieve lattice mismatch stress corresponds to a 0.1 % deformation. This is an upper limit since we expect the film to be under slight compression at the growth temperature. With a density of $\geq 4 \times 10^8$ cm^{-2} of TDs that can glide to relieve mismatch strain, each dislocation would only have to move ≤ 2-3 μm to produce a 0.1 % deformation through reduction of the average MD length at the interface. This is consistent with our earlier conclusion from the TEM observations that the TDs move ≤ 3 μm during cool down from the growth temperature. When the structure is heated to 850 °C and subsequently cooled the TDs have to move at least twice as far in both the reverse and forward directions to accommodate the thermal mismatch cycling. At 850 °C the dislocation mobility is also much higher than at the growth temperature. With the present TD densities this leads to dislocation interactions which result in an entangled appearance of the TDs in the top layer of the post growth annealed films as observed.

Figure 6 shows a cross section of a GaAs film on a Si mesa. It shows a high density of entangled dislocations near the interface. This is indicative of intense dislocation interaction and a high TD density during the early stages of growth. It is during this stage that most of the plastic relaxation of the 4% mismatch strain occurs and it is potentially the stage when TDs could move long distances. However, since the dislocation density is then several orders of magnitude higher than during later stages, and since the average distance TDs have to propagate to produce a given amount of plastic relaxation decreases with increasing TD density, it is plausible that most TD segments move only a short distance during this stage as well as during later stages when the relaxation process has slowed down. The dislocation density decreases rapidly during the early growth stage because dislocation reactions lead to

annihilations and combination of TD segments. In this scenario the TD structure and density is determined by frequent interactions between TDs and is not affected by the size of the growth area when this has dimensions of several µm.

C. GaAs on Si with a ZnSe interlayer and ZnSe on Si

From the cross section in Fig. 6 one can see that the entanglement of the TDs at the interface could impede their motion during cool down and limit the plastic relaxation. We tried to enhance the mobility of the dislocations near the interface by growing a plastically softer interlayer of ZnSe between the Si and the GaAs. ZnSe and GaAs have similar lattice parameters and thermal expansion coefficients but GaAs has a hardness that is 5 times larger than that of ZnSe. The lower hardness of ZnSe suggests that it has a higher dislocation mobility. The increased dislocation mobility was anticipated to increase the relaxation of the film, i.e. lower strain in the as-grown film at room temperature. It was also hoped that it would facilitate termination of dislocations at the mesa edges and hence reduce the TD densities. A previous study by Lee et al[9], using etch pit density and photoluminescence, indicated a decrease in both strain and dislocation density for GaAs grown on a ZnSe interlayer. In our investigation, however, the residual strain in the GaAs layer grown on a ZnSe interlayer on continuous substrates as measured by XRD was the same as without the interlayer. The TD density was also the same with and without the ZnSe interlayer both on patterned and unpatterned substrates. We also studied a 2 µm ZnSe film on Si. This film exhibited an in-plane tensile strain of 0.08 % and a TD density similar to that of a GaAs film. This means that despite the difference in hardness at room temperature we do not observe a significant difference between ZnSe and GaAs with respect to the amount of residual strain in the films. Dislocation mobilities decrease rapidly with decreasing temperature and the residual strain depends on the "freeze-in temperature" at which dislocations become immobile

during cool down. The dislocation mobility in GaAs depends exponentially on 1/T and decreases by more than 2 orders of magnitude when the temperature decreases from 300 to 200° C[10]. In view of the strong dependence of dislocation mobility on temperature it is possible that the difference in mobility anticipated from a factor of 5 difference in hardness is still too small to significantly change the freeze-in temperature.

IV. SUMMARY

We have shown strong evidence that the difference in thermal expansion coefficient between Si and GaAs is not a dominant source of the TDs that are observed in as grown GaAs films on Si. It was also found that TD densities were unaffected by reduction in growth area down to our smallest mesa size of 10 μm. A previous investigation of GaAs growth on Si mesas showed a reduction in etch pit density with reduced mesa size[11]. This different result may be due to the possibility that the etch pit density, which relies on strain fields around dislocations[12], does not truly reflect the TD density in this case, since the residual strain in the film decreased with decreasing mesa size. We suggest that the direct reason for the non-dependence of TD density on growth area in our measurements is that the threading dislocations do not move far enough to interact with the edges during any stage of growth or cool down. To test if free sidewalls can pin dislocations we are further investigating the combination of reduced area growth with additional strained layers which force the TDs to propagate over longer distances.

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Figure captions

Fig.1. Process for fabrication of Si mesas with overhanging sidewalls.

Fig.2 Procedure for preparation of large area plan-view TEM specimen.

Fig.3. TEM plan-view micrograph from a 2 μm thick GaAs film on a Ge(001) substrate (off-cut 4° toward [1$\bar{1}$0]). The diffraction vector was a <220> near the [001] zone.

Fig.4. TEM plan-view images of the top ~0.4 μm of a 2 μm thick GaAs film on 24 μm wide Si mesas: (a) as-grown, (b) after anneal to 850 °C for 15 min.

Fig.5. TEM plan view of an as-grown GaAs film on a 10 μm Si mesa. Both micrographs show the same areas using g=$\bar{2}$20 in the top panel and g=400 in the lower near the [001] zone. Threading dislocations associated with glissile misfit dislocations are indicated by G and threadings associated with sessile misfits by S.

Fig.6. TEM cross section of an as-grown GaAs film on a 10 μm Si mesa. The diffraction vector was a <220> near a <110> zone.

SiO$_2$

1. Grow and pattern 350 nm oxide on a Si wafer.

Si
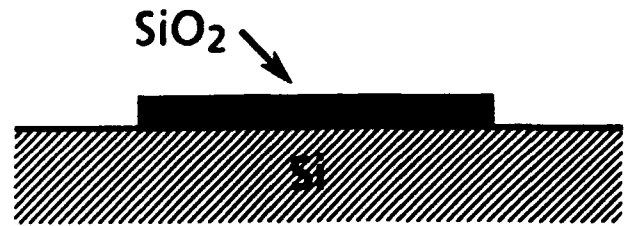
2. Etch in CF$_4$ plasma.

3. Grow 70 nm oxide in the vias.

Ion bombardment helps etch SiO$_2$
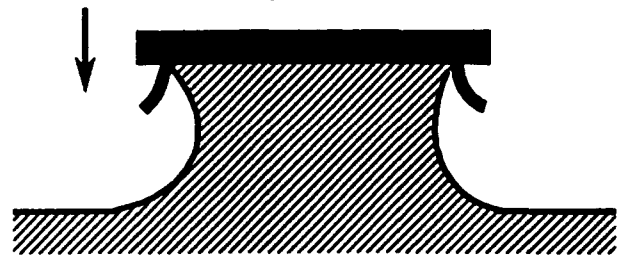
4. Etch in CF$_4$ plasma

5. Remove oxide in HF

Polyimide

GaAs

1. Spin polyimide on sample.
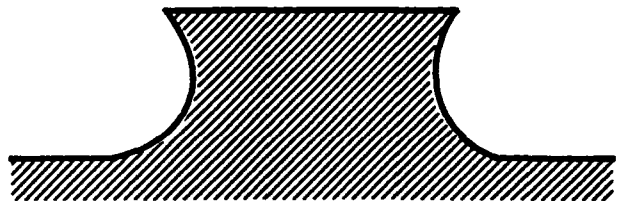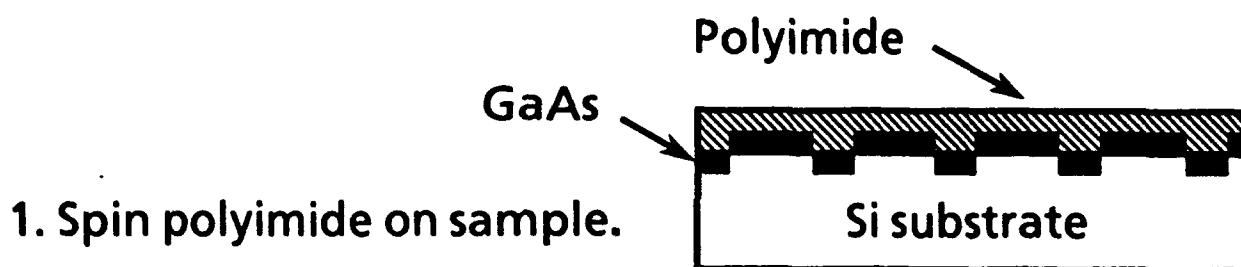
Si substrate

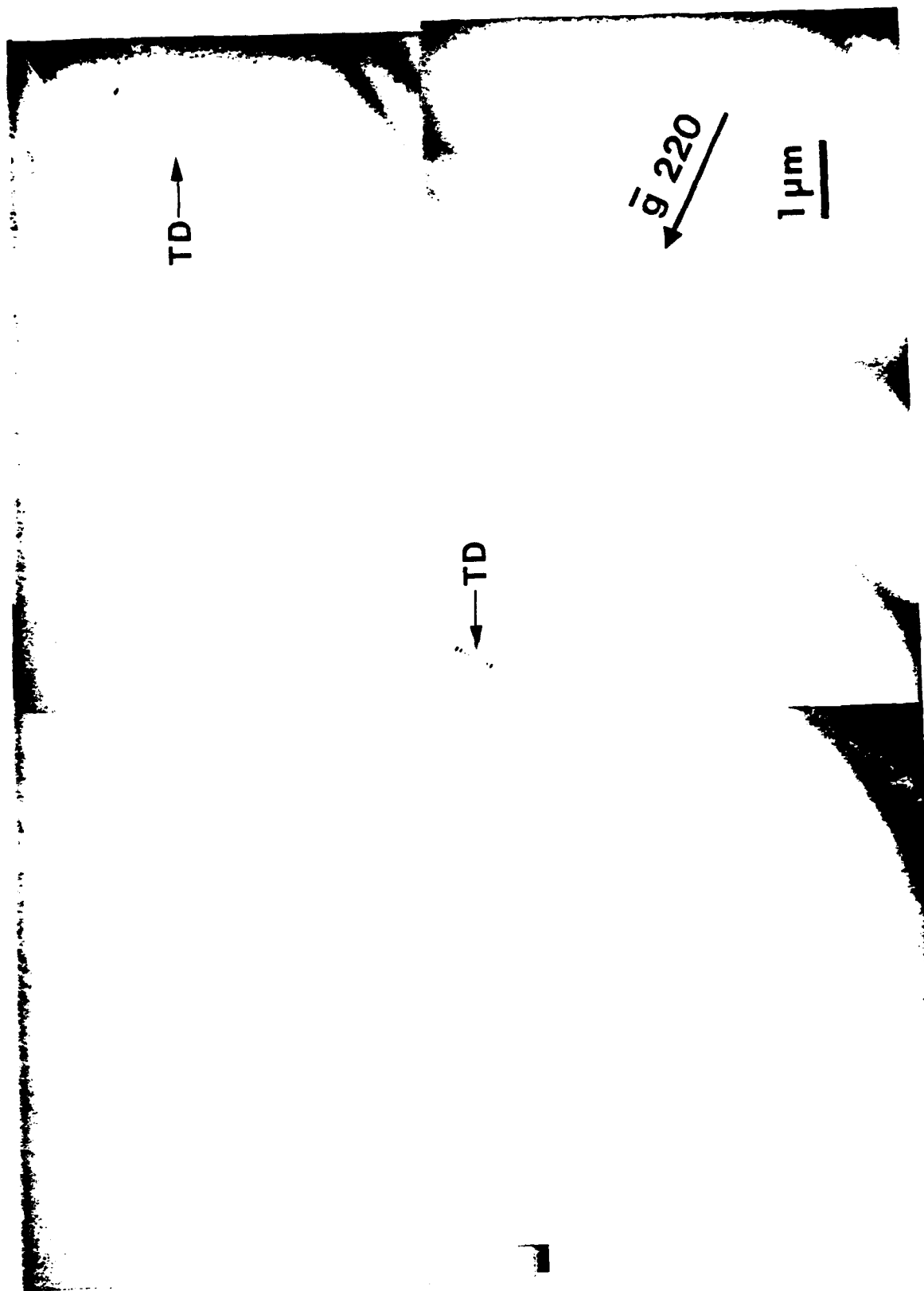**2. Cut 3 mm disc and dimple from substrate side.**

3. Plasma etch with CF$_4$ from substrate side.
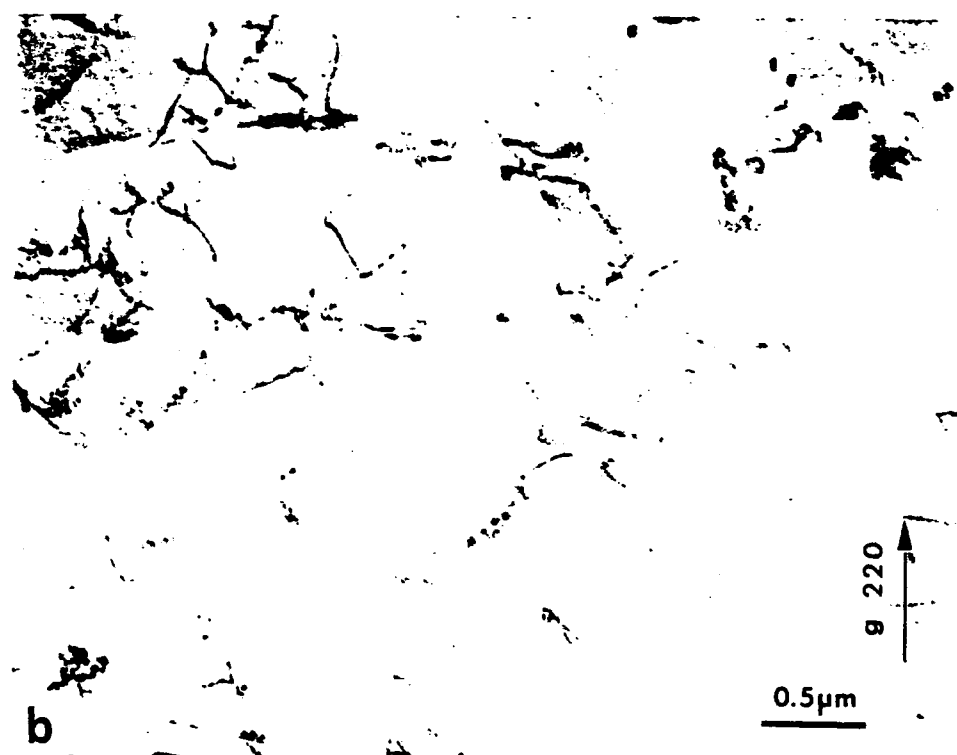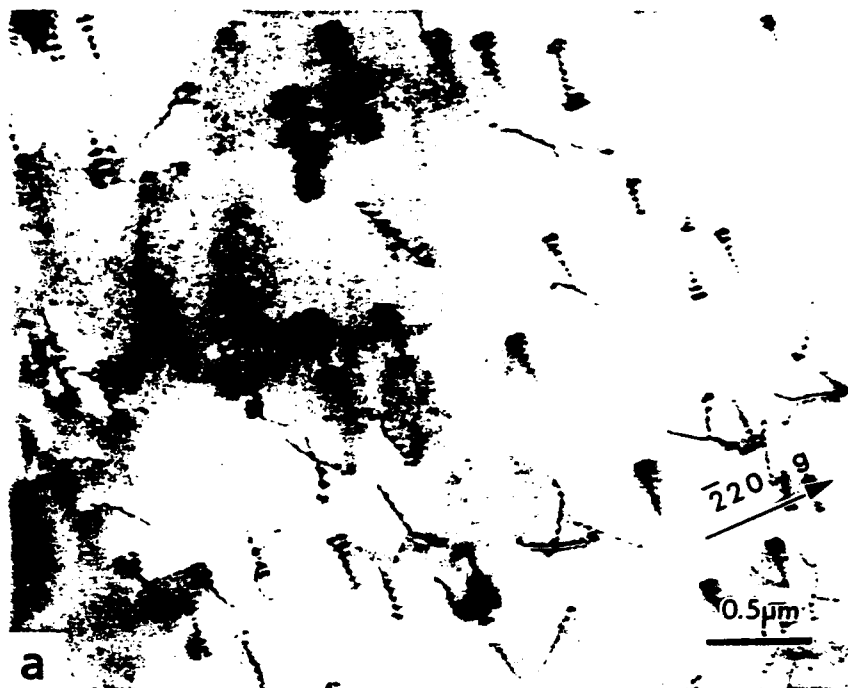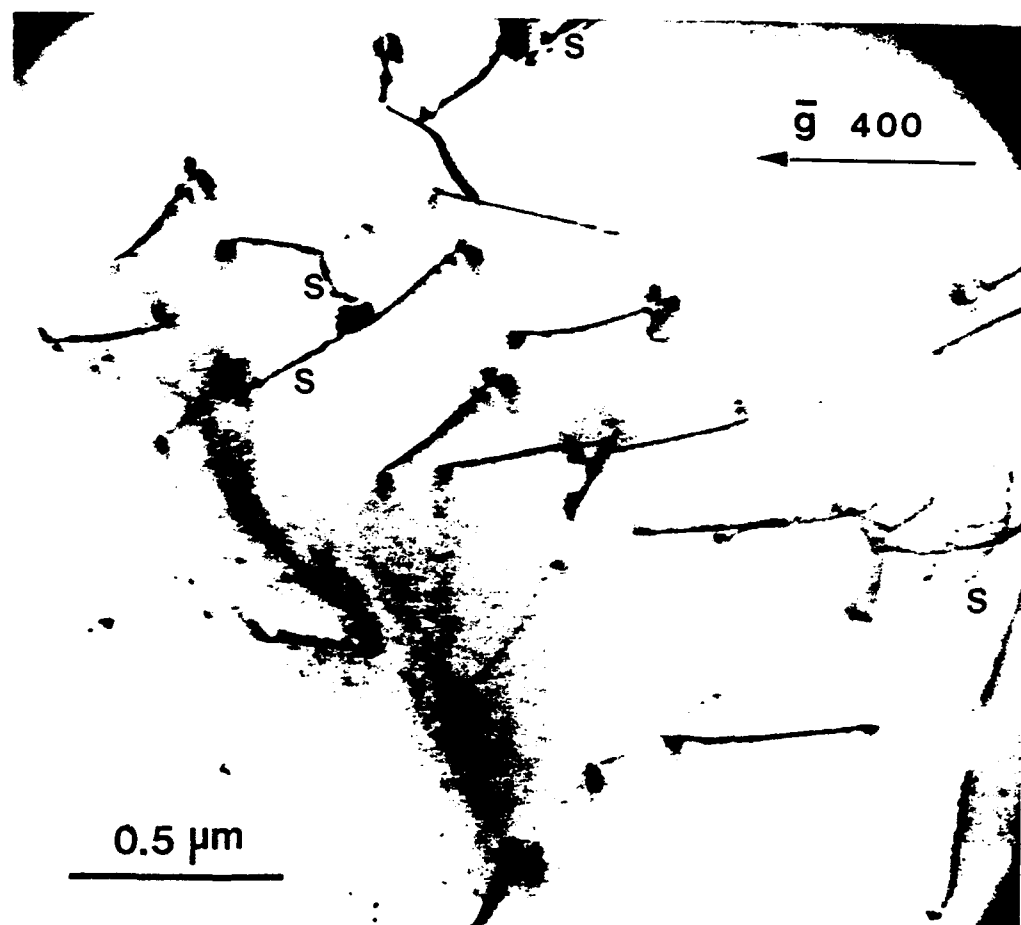
4. O$_2$ plasma etch polyimide

e-beam transparent mesa
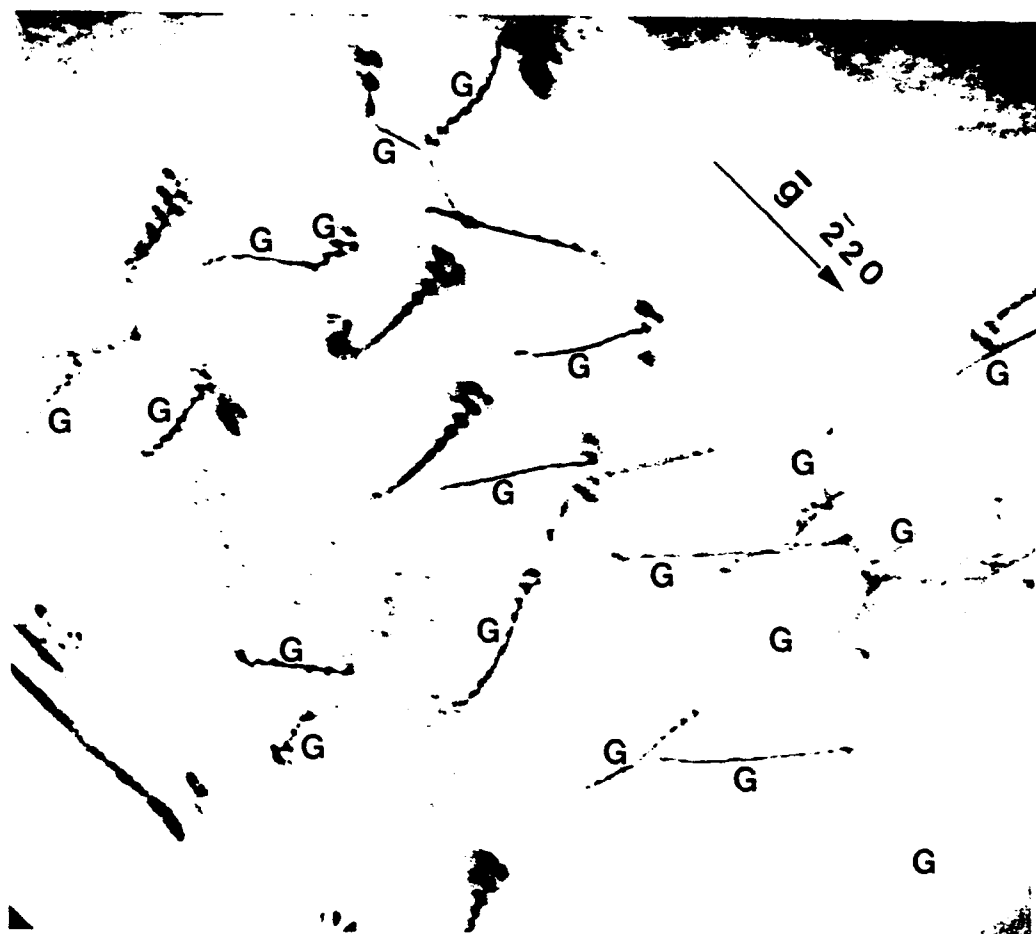
5. Ion mill from substrate side.

TD→

TD

g̅ 220

1 μm

a

$\overline{2}20$ g

0.5μm

g 220

0.5μm

b

g̅ 2̅2̅0

g̅ 400

0.5 μm

g (1220)

1 μm
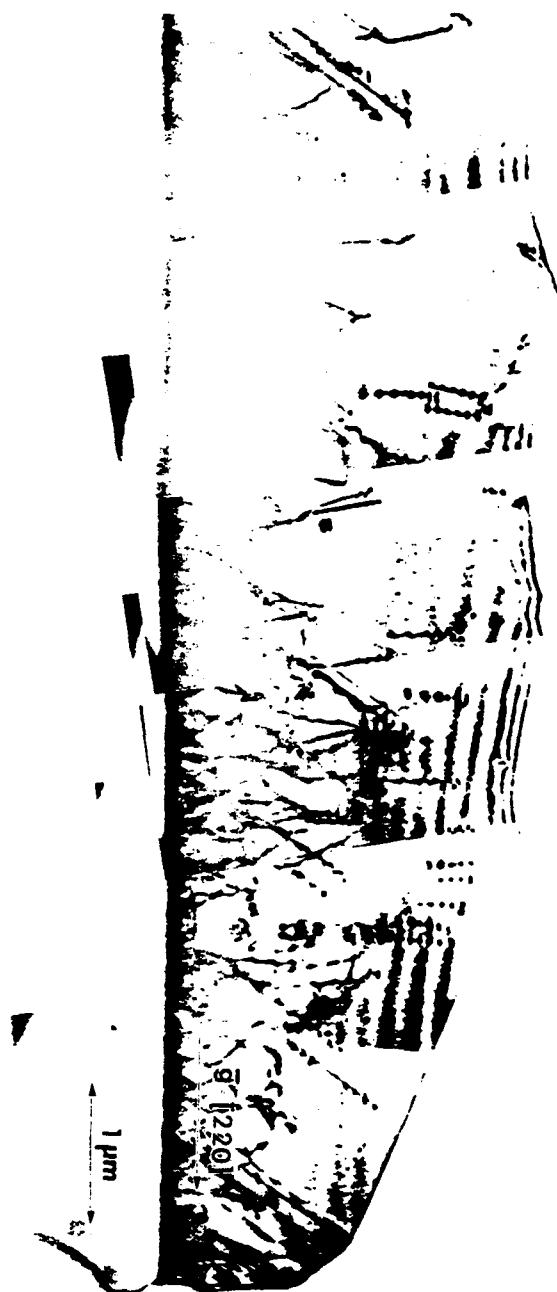
The use of graded InGaAs layers and patterned substrates to remove threading dislocations from GaAs on Si

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Abstract

We have investigated threading dislocation (TD) removal from GaAs films on Si by introduction of additional InGaAs graded strain layers in combination with growth on patterned substrates. The substrate patterns consisted of mesas with 10-34 μm widths. The mesa sidewalls were either overhanging (concave), leading to free sidewalls for the film on the mesas, or outward sloping (convex) sidewalls with {111} orientation. The dislocation structure was studied using transmission electron microscopy. It was found that the graded strained layers led to a reduction of dislocation density by a factor of ~5 in films grown both on mesas with concave sidewalls and on unpatterned substrates. This reduction was due to dislocation reactions leading to annihilation of TDs. An additional factor of ~3 reduction in TD density was achieved for films with graded strained layers on mesas with convex sidewalls. In this case all mobile TDs (TDs associated with 60° misfit dislocations i.e. TDs that could glide to relieve misfit stress) were removed from the film on the mesas and only TDs associated with 90° misfit dislocations remained. We suggest that this is due to pinning of the TDs at the mesa edges and have presented an explanation for this pinning in terms of the stress conditions at the {111} oriented mesa edges. In addition this leads us to suggest that in order to obtain minimum TD

density it is imperative to prevent formation of 90° misfit dislocation during lattice mismatched heteroepitaxial growth.

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I INTRODUCTION

In a recent publication Fitzgerald et al[1] have shown that heteroepitaxial growth on reduced area mesa structures leads to a reduction both in misfit dislocation (MD) and threading dislocation (TD) densities for systems with moderate lattice mismatches of < 0.4%. However, for GaAs on Si, which has a 4% mismatch, it has been found that reduced area growth does not lead to reduced TD densities[2]. This was in part attributed to the finding that TDs do not move during growth over long enough distances to encounter an edge. The average distance that TDs move, and hence the probability of interactions between edges and TDs, can be increased by additional lateral forces. Strained layers, for example, can deflect dislocations so that they propagate parallel to the interface plane. Strained layers and superlattices have previously been applied in the quest for lower threading dislocation densities in the GaAs on Si system[3-8] and other lattice mismatched heteroepitaxial systems[9-13]. However, the intuitively very promising combination of patterned substrates with strained layers has only been summarily reported by Sohn et al[14]. The reduction of TD densities by a strained layer can proceed through several mechanisms. Figure 1 depicts five situations that can occur when a TD encounters a layer with a different equilibrium lattice parameter[15]. In case (ı), the mobility of the dislocation is so low that the dislocation appears unaffected by the strained layer. This situation also occurs if the Burgers vector b of the dislocation is such that the layer strain does not exert a net lateral force on the dislocation. In situation (ıı) the TD bends and reacts with another dislocation to form a single threading segment. Case (ııı) occurs as a special case of (ıı) when the sum of the Burgers vectors of the reacting dislocations is zero and the threading segment is annihilated. In case (ıv) the dislocation bends and propagates parallel to the interface for some distance and then bends up again and threads to the surface. Situation (v) occurs

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when the dislocation bends and terminates at a film edge and does not thread through the layer to the top surface. Mechanisms (ii) and (iii) are efficient in reducing the TD density at high dislocation densities but their efficiency is dramatically reduced as the TD density decreases. For maximum dislocation reduction it appears that we also have to rely on mechanism (v). Growth on reduced area structures then becomes useful to make it easier for dislocations to terminate at edges. Termination of a dislocation at a free film edge is energetically favorable and the edge will therefore provide some pinning of the dislocation. However, it is possible that there are other type film discontinuities which intervene or are, in fact, more efficient in pinning dislocations. In the present paper we report on an investigation in which InGaAs strained layers were used in combination with patterned substrates. We have studied how effective the strained layers are in deflecting TDs with different Burgers vectors. Graded and abrupt changes in lattice parameter were used to probe the effect of dislocation interactions. We have also compared the dislocation pinning efficiency of two types of film discontinuities by growth on two types of mesas (see fig. 2): (i) mesas with concave sidewalls which lead to overgrown layers with free sidewalls versus (ii) convex mesas with {111} oriented sidewalls which produce a segment of a continuous film with different surface orientation and different strain configuration.

II EXPERIMENT

Both molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) were used for growth of films. The first layer always consisted of ≥500 nm of GaAs grown by MBE where the first 100 nm was deposited at a substrate temperature (T_s) of 400 °C and subsequent GaAs layers at $T_s = 600$ °C. MOCVD growth was carried out at $T_s = 750$ °C. For surface protection during transfer

from the MBE to the MOCVD reactor the MBE layers were capped with a layer of amorphous As.

The Si substrates were cut so that their surface normals were tilted 4° from [001] towards the [1$\bar{1}$0] direction. We have grown on Si mesas with two different sidewall profiles (see fig. 2); (i) concave (overhanging) sidewalls and (ii) convex (outward sloping) side walls with {111} orientation. The concave sidewalls were obtained by a two step plasma etch and oxidation process[2] and the {111} oriented sides were produced by etching in a solution of 30 wt.% KOH in H_2O at a temperature of ~80° C using an SiO_2 pattern on the substrate to define the mesa tops. The SiO_2 mask was subsequently removed with HF.

Three types of GaAs/InGaAs structures were grown. The In concentration versus thickness profiles for these structures are shown in fig. 3. Structure (A) started with growth of ~1 μm GaAs by MBE. The remainder of the structure was grown by MOCVD and consisted of a graded InGaAs layer with the In concentration increasing linearly from 0 to 15 % over a thickness of ~1.7 μm followed by a ~0.5 μm $In_{0.15}Ga_{0.85}As$ layer. An In concentration of 15% gives a ~1% larger lattice parameter than GaAs. Structure (B) was produced in a similar fashion but the In concentration was only increased to 10% and then graded back down to 0%, and the top layer consisted of GaAs. Structures (A) and (B) were deposited both on mesas with overhanging sidewalls and mesas with {111} oriented side walls as well as on unpatterned substrates. Structure (C) was entirely grown by MBE and contained abrupt changes in In concentration as well as graded layers. (The purpose of the abrupt changes was to increase the dislocation interactions.)

The films were studied by cross-sectional and plan-view transmission electron microscopy (TEM). To allow for large area viewing, the plan-view samples were prepared by a technique that relies on selective plasma etching of the substrate[2].

Cross-sections were prepared by traditional mechanical dimpling and argon ion milling.

III RESULTS AND DISCUSSION

A. Threading Dislocation Density

A cross-sectional TEM image of structure (B) grown on a 34 μm wide mesa with concave sidewalls is presented in fig. 4. It is evident that the graded strain layers indeed bend many of the TDs into MD segments and that the TD density is decreased. Due to the finite In concentration gradient, the MDs are distributed over some depth within the graded layers. If we look at this sample in plan view (see fig. 5) we observe that the TD density (ρ_{TD}) is 12×10^7 cm-2. This is a substantial reduction when compared to the density of 70×10^7 cm-2 found for pure GaAs on Si grown under otherwise identical circumstances[2]. (Table 1 gives an overview of the TD densities measured for the different substrate/film combinations that were investigated.) Similar reductions in TD densities were observed for structure (B) grown on a continuous substrate ($\rho_{TD} \approx 9 \times 10^7$ cm-2) and for structure (A) on both concave mesas ($\rho_{TD} \approx 12 \times 10^7$ cm-2) and continuous substrates ($\rho_{TD} \approx 13 \times 10^7$ cm-2). Structure (C) exhibited a somewhat smaller reduction in TD density. The fact that the reductions in TD density obtained in the cases described above are the same for both continuous substrates and mesas with concave sidewalls shows that free sidewalls during growth are not effective in reducing the TD density. The reductions are thus mainly due to dislocation reactions that lead to annihilations and combination of TDs (events II and III in fig. 1). In contrast, an additional reduction in ρ_{TD} to $4-5 \times 10^7$ cm-2 was detected in both structure (A) and (B) when grown on mesas with {111} oriented sidewalls (see fig. 6). In this case the sidewalls reduce the

TD densities and it is likely that mechanism V in Fig. 1 is active. Further evidence of this was obtained from Burgers vector analysis for the TDs.

B. Analysis of Dislocation Behavior

We have analyzed the Burgers vectors of the TDs by recording plan-view TEM images in four different two-beam conditions using diffraction vectors g = (040), (400), (220) and (2$\bar{2}$0). The requirement to accurately maintain the same diffraction condition throughout an image is more stringent when performing b analysis than it is when only a TD density is required, so a smaller field of view must be used. We typically recorded images from two different areas from each sample, containing a total of 20-30 dislocations. In zincblende structure materials dislocations generally have Burgers vectors along <110> directions and glide on {111} planes. This means that two types of misfit dislocations can exist at a (001) interface; 90° dislocations, which are sessile and have bs that lies in the interface plane, and 60° dislocations, which are glissile and have bs out of the interface plane. A 60° misfit can change its length during plastic relaxation by glide of the corresponding threading segments whereas the 90° MD can only change its length by climb of the TDs. Glide is a much faster process than diffusion-limited climb which means that TDs with in plane bs will move much more readily in response to a mismatch strain than TDs with in plane bs[11]. In the presence of both types of TDs we thus expect glide of TDs with out of plane bs to be the dominant mechanism for plastic deformation. TDs associated with sessile MDs have b = ±a/2[110] or ±a/2[$\bar{1}$10] and will be referred to as S-type TDs in the following. TDs associated with glissile MDs have b = ±a/2[101], ±a/2[$\bar{1}$01], ±a/2[011] or ±a/2[0$\bar{1}$1] and are called G-type. Dislocations with $g·b$ = 0 show reduced contrast in a TEM image, so from our series of pictures with different gs we can distinguish between G- and S-type TDs.

Figure 7 shows an example of two images obtained with different g vectors from the same area of a film with structure (A) on a continuous substrate. The dislocation types are indicated in the figure. We see that about two thirds of the dislocations are associated with glissile MDs and one third with sessile MDs. This result was found to be typical of all InGaAs/GaAs structures grown on continuous substrates and on mesas with overhanging sidewalls. For films on mesas with convex {111} sidewalls the situation was different and essentially no G-type TDs were observed. The G-type TDs respond to the strain induced by the InGaAs layers by gliding laterally to form a MD segment. S-type TDs are unable to respond in this way and remain immobile. The removal of all mobile TDs from the interior (away from the edges) of mesas indicates that {111} sidewalls are effective in pinning the TDs as they try to move across the sidewalls.

From stereoscopic crossectional TEM images of the edges we have found that many 60° MDs which approach an edge turn and propagate along a direction that lies in the {111} plane with the same orientation as the edge of the mesa. In the crossectional view of an edge shown in fig. 8 this gives the appearance of a number of dislocations that seem to bend down towards the substrate as they approach the edge (indicated by arrows in Fig. 8) or just end (turn in a direction perpendicular to the image plane) before they reach the edge. A schematic view of this behavior is shown in Fig. 9. The bending effect is understandable in terms of the strain conditions at the edge. During growth of the graded InGaAs layer the TD motion is driven by compressive biaxial strain. In the interior of a mesa the compression is oriented in the (001) plane whereas at the edges the strain is oriented along a {111} plane which is at an angle of 55° to the (001) plane. After the MD has turned to extend along a direction in a {111} plane it relieves the misfit strain of this interface. TDs that can glide to relieve the misfit stress of the (001) interface (G type TDs) have

b = ±a/2[101], ±a/2[$\bar{1}$01], ±a/2[011] or ±a/2[0$\bar{1}$1], and the driving force for their motion is provided by the resolved shear stress τ which is the shear stress in the glide plane resolved along **b**[16]. For a misfit stress on the (001) plane τ is nonzero for all these **b**s. However, for misfit stress on a {111} interface plane τ is zero for those **b**s that lie in the interface plane. Let us consider four possible TDs with **b** = a/2[101], a/2[10$\bar{1}$], a/2[0$\bar{1}\bar{1}$] and a/2[0$\bar{1}$1] gliding and extending their MD segments along the [110] towards a (111) oriented mesa edge. (The choice of [110] as the line direction for the MDs eliminates the ± option on the Burgers vectors since we consider the topmost layer to be in compression). On the (111) oriented interface τ will be zero for the dislocations with **b** = a/2[10$\bar{1}$] and a/2[0$\bar{1}$1]. This means that the driving force for glide motion of the threading segment with these **b**s will vanish as they begin to move across the (111) oriented mesa edge, and it is clear that the mesa edge will constitute a significant obstacle for the propagation of these TDs.

That most MDs appear to bend into the (111) plane at the edge may be due to the possibility that the strain condition at the mesa edge facets is not purely {111} oriented and there could still be a small remanent driving force for glide that could move the dislocation partially across the mesa edge. In addition there is still a significant climb force on these dislocations and we can not completely exclude the possibility that climb plays some role in extending the dislocation small distances along the (111) interface. The TDs that have **b**= a/2[101] and a/2[0$\bar{1}\bar{1}$] can glide across the (111) oriented mesa edge. After gliding to the neighboring mesa (~5μm away), however, they will encounter an edge with ($\bar{1}\bar{1}$1) orientation and become pinned in analogy with the above discussion. It should also be mentioned that previous investigations by Watson et al[17] have suggested another mechanism for hindrance of TD propagation across inclined mesa edges. That mechanism is based on the line tension of the threading which will resist extension of the TD as it reaches

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the mesa edge. However, it relies on the assumption, unsupported here, that the TD maintains a specific line direction.

The density of 4-5x10^7 cm^{-2} S-type TDs obtained for the InGaAs/GaAs structures on mesas with {111} sidewalls is significantly lower than the density of such TDs in a pure GaAs film grown under otherwise similar conditions. This shows that the graded strained layers have reduced also the density of S-type TDs. Despite being virtually immobile, these dislocations can be transformed to mobile G-type TDs by reactions with mobile dislocations and then annihilated by a second reaction. Corr ondingly they can also be formed by reactions between G-type TDs with Burg vectors that sum up to an in-plane b.

Figure 10 shows a part of the misfit dislocation network of structure A on a mesa with {111} sidewalls. We are looking only through the top InGaAs layer with constant In concentration and part of the adjacent graded InGaAs layer, with the underlying layers having been removed during the specimen preparation. We see a dislocation network consisting of a majority of 60° MDs and a small minority of 90° MDs. (Each 90° MD goes out of contrast completely for one or the other of the two g conditions used in the two micrographs. A few 90° MDs are marked by arrowheads in fig. 10.) We suggest that the observed 90° MDs are formed by combination of two 60° MDs with Burgers vectors that add up to produce a b lying in the surface plane. This reaction can proceed by glide of a G-type TD along a preexisting 60° MD[18].

IV SUMMARY

It has been found that graded InGaAs layers reduce the density of threading dislocations associated with both sessile and glissile misfit dislocations of the GaAs/Si interface. The reduction proceeds through dislocation interactions leading to

annihilation and combination. Mobile TDs can be completely removed from films grown on convex mesas with {111} sidewalls. Despite the fact that the TD densities are still high this is an encouraging result as it shows that the thermal mismatch between Si and GaAs is not a severe source of TDs. TDs that would conceivably be associated with the thermal mismatch would be mobile and can thus be removed. Another conclusion is that to obtain completely TD-free films it is important to suppress formation of 90° MDs and their immobile TD segments. This could possibly be accomplished by continuously grading the lattice parameter from that of Si to that of GaAs by using a graded Si/Ge buffer layer. Such a procedure would maintain 2D layer growth and would minimize dislocation interactions. Encouraging results from the use of a graded Si/Ge buffer layer on continuous substrates have recently been reported by Fitzgerald et al[13]. A combination of such a buffer layer with growth on mesas with {111} sidewalls has a very high potential for producing presently unattained low TD densities.

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Figure captions

Fig.1. Possible dislocation configurations that can occur when a lattice mismatched layer is deposited on a layer which contains threading dislocations.

Fig.2. Schematic cross-sectional view of the two types of mesas that were patterned into the substrates.

Fig.3. Indium concentration versus thickness profiles for the three structures grown.

Fig.4. Cross-sectional TEM image of structure (B) grown on a 34 μm wide mesa with concave sidewalls.

Fig.5. TEM plan-view image through the top 0.2-0.3 μm of structure (B) grown on a 34 μm wide mesa with concave sidewalls.

Fig.6. TEM plan-view image through the top 0.3-0.4 μm of structure (A) grown on a 24 μm wide mesa with convex {111} oriented sidewalls. The large extended defect in the lower right is a stacking fault. Stacking faults are only occasionally observed in our films.

Fig.7. TEM plan view through the top ~0.3 μm of structure (A) grown on a continuous Si substrate. Both micrographs show the same areas using $g=220$ in the top panel and $g=400$ in the lower near the [001] zone. Threading dislocations associated with glissile misfit dislocations are indicated by G and threadings associated with sessile misfits by S.
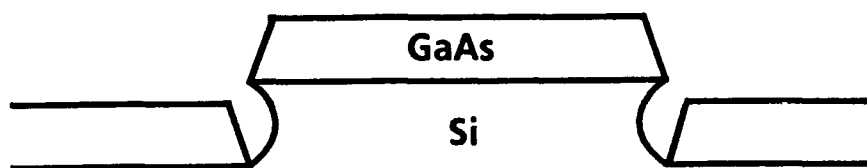
Fig.8. Cross-sectional TEM image near a mesa edge of structure (A) grown on a 34 μm wide mesa with convex sidewalls. Many dislocations are seen to bend into the (111) plane that is parallel to the mesa side.

Fig. 9. Schematic drawing of dislocations that change direction near a mesa edge. The misfit dislocations depicted here are located near the interface between the InGaAs and the GaAs. When they reach the mesa edge they follow the (111) oriented interface plane, then thread to the film surface and terminate.
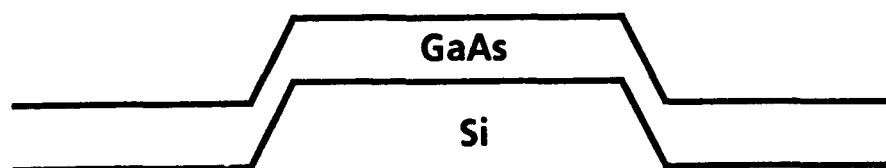
Fig. 10. Plan view TEM images from structure (A) on a 24 μm wide mesa with convex {111} oriented sidewalls. The images are projections through top the InGaAs layer and part of graded InGaAs layer below. The graded InGaAs layer contains a network of misfit dislocations. The arrow heads point to 90° misfit dislocations. Both micrographs show the same areas using $g=2\bar{2}0$ in the left panel and $g=220$ in the right near the [001] zone.
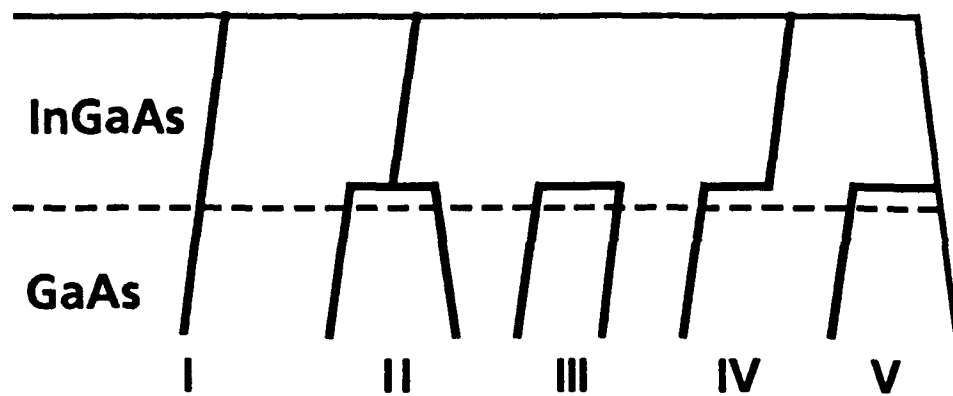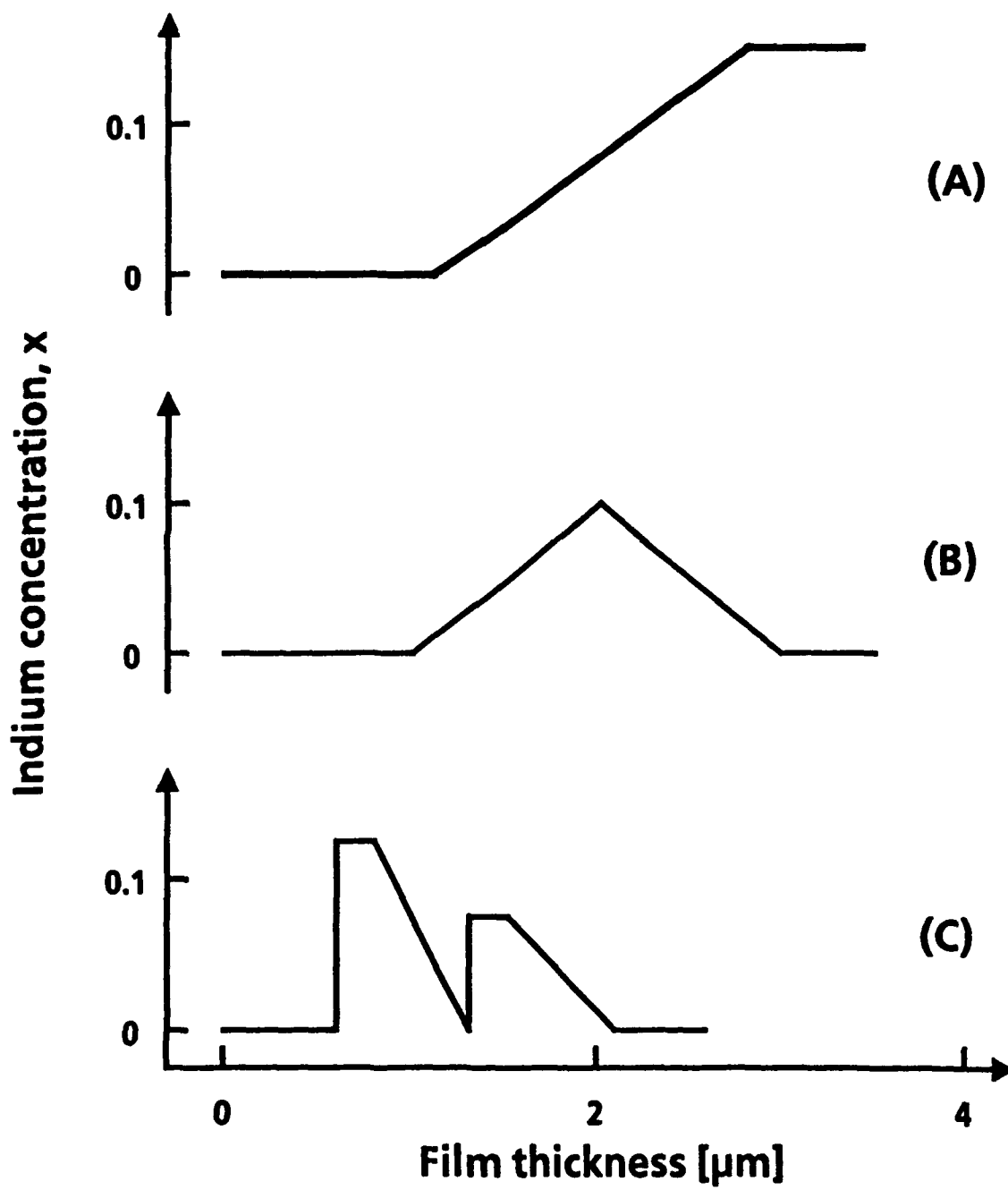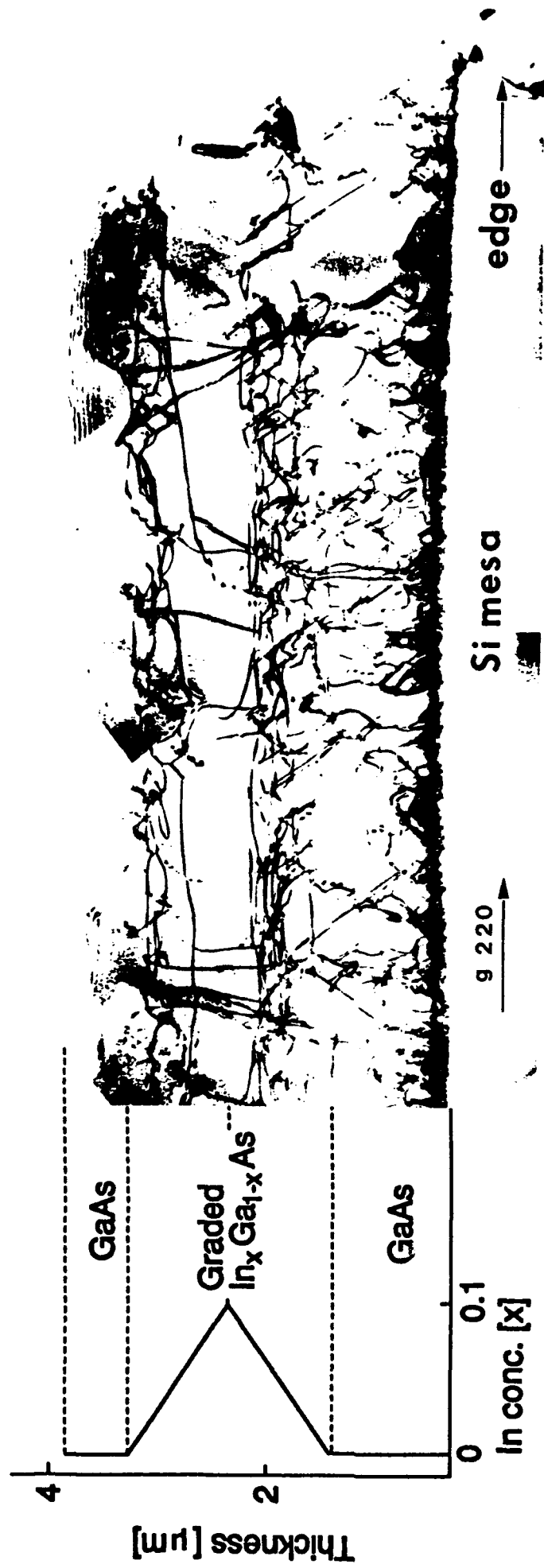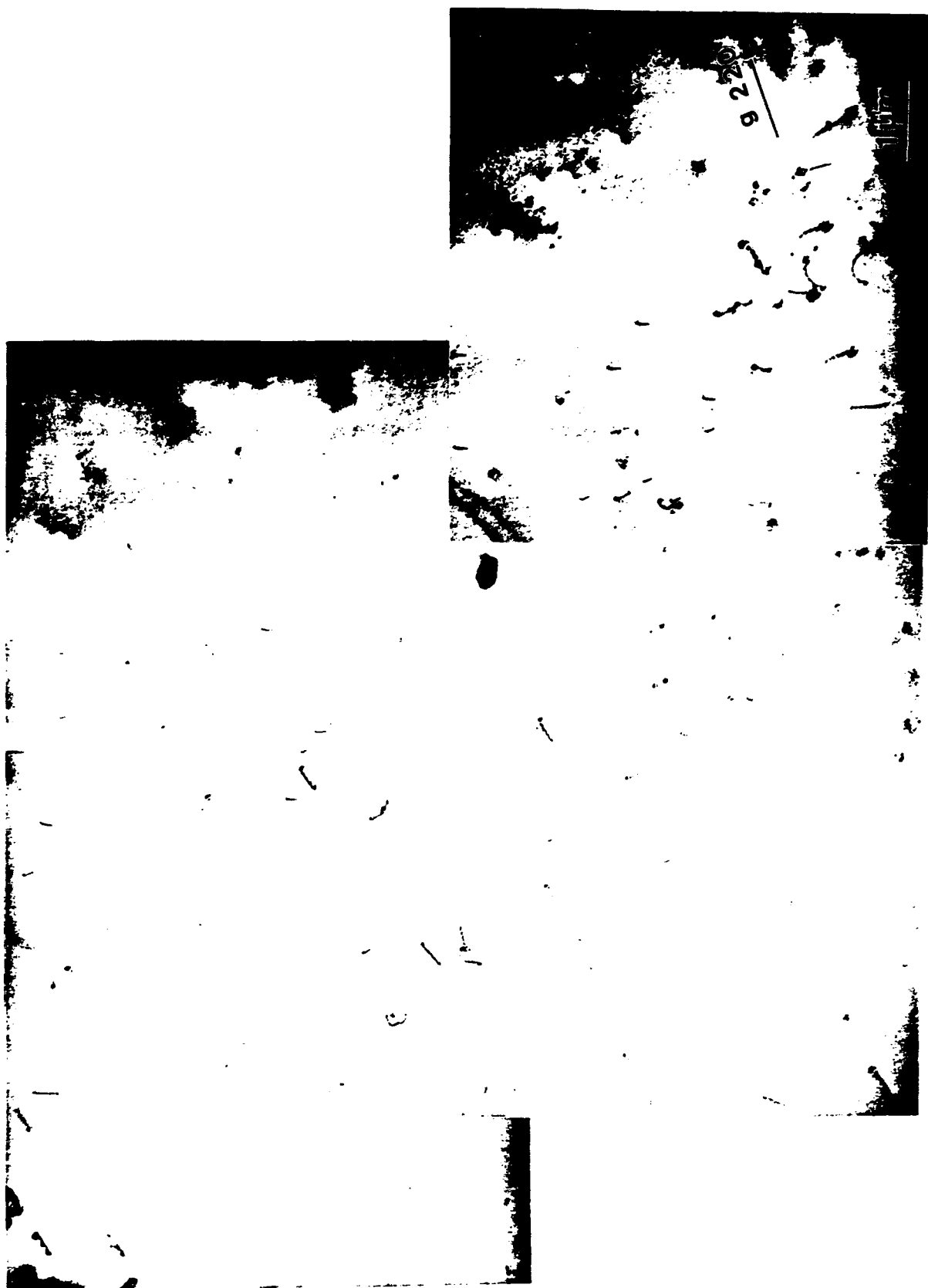
InGaAs

GaAs

I II III IV V

Mesa with concave sidewalls

GaAs

Si

Mesa with convex {111} sidewalls

GaAs

Si

edge

Si mesa

g 220

GaAs

Graded
In$_x$Ga$_{1-x}$As

GaAs

In conc. [x]

0.1

0

4

2

Thickness [μm]

g 220

1 μm

Film edge

In$_{0.15}$Ga$_{0.85}$As

Graded InGaAs

GaAs

AlAs

g 004

1 μm

Si mesa

MD on (001)

MD on (111)

TD

InGaAs

GaAs

Si

[001]

[110]

[1$\bar{1}$0]

g 220

1 μm
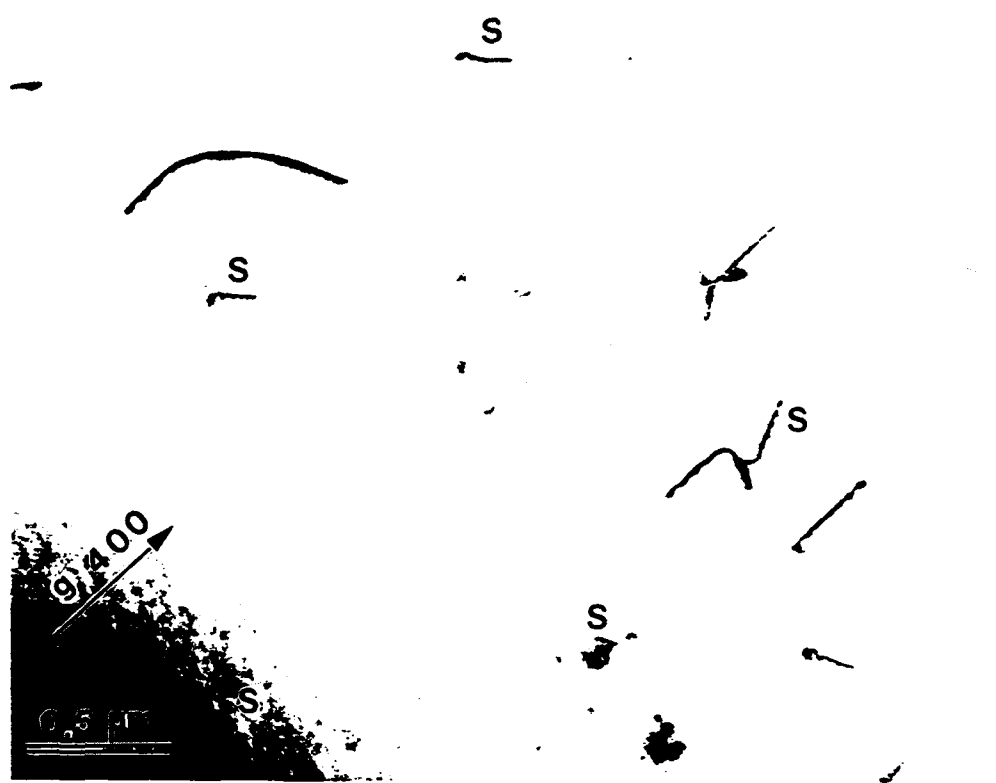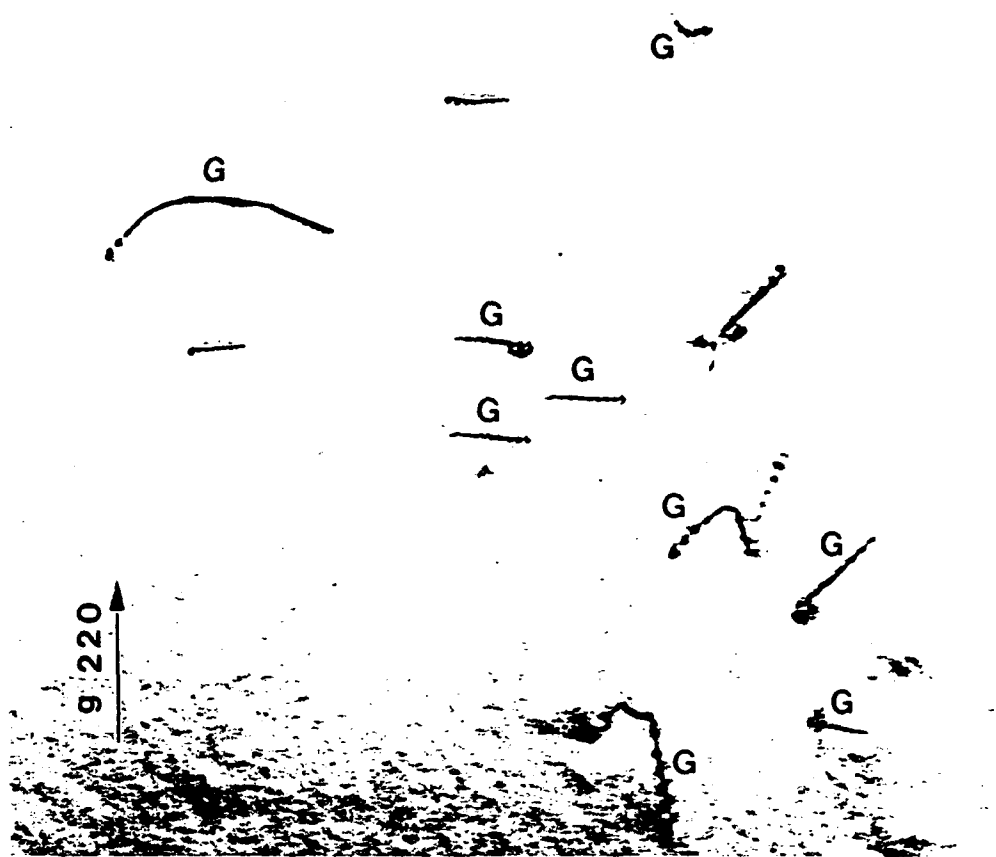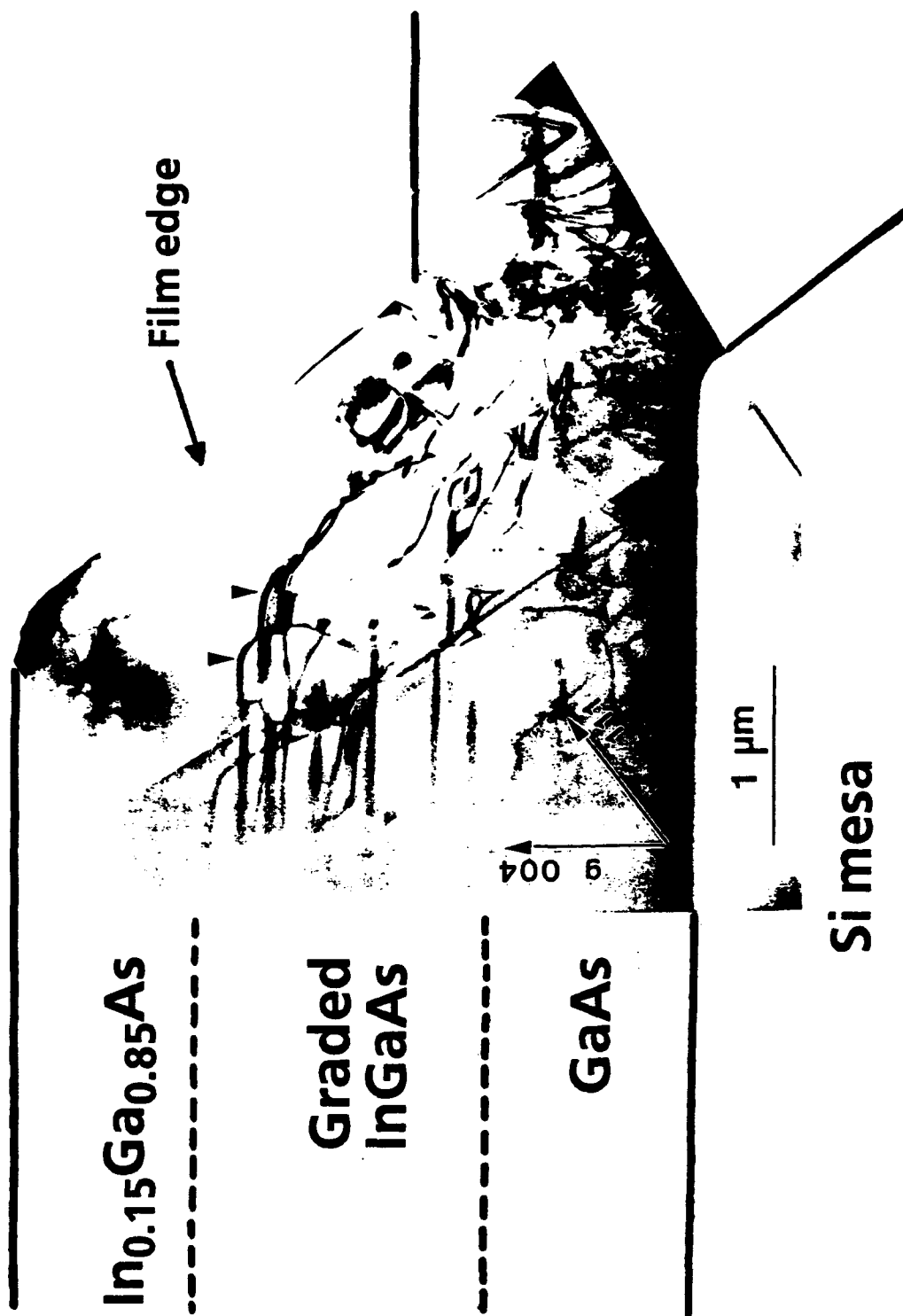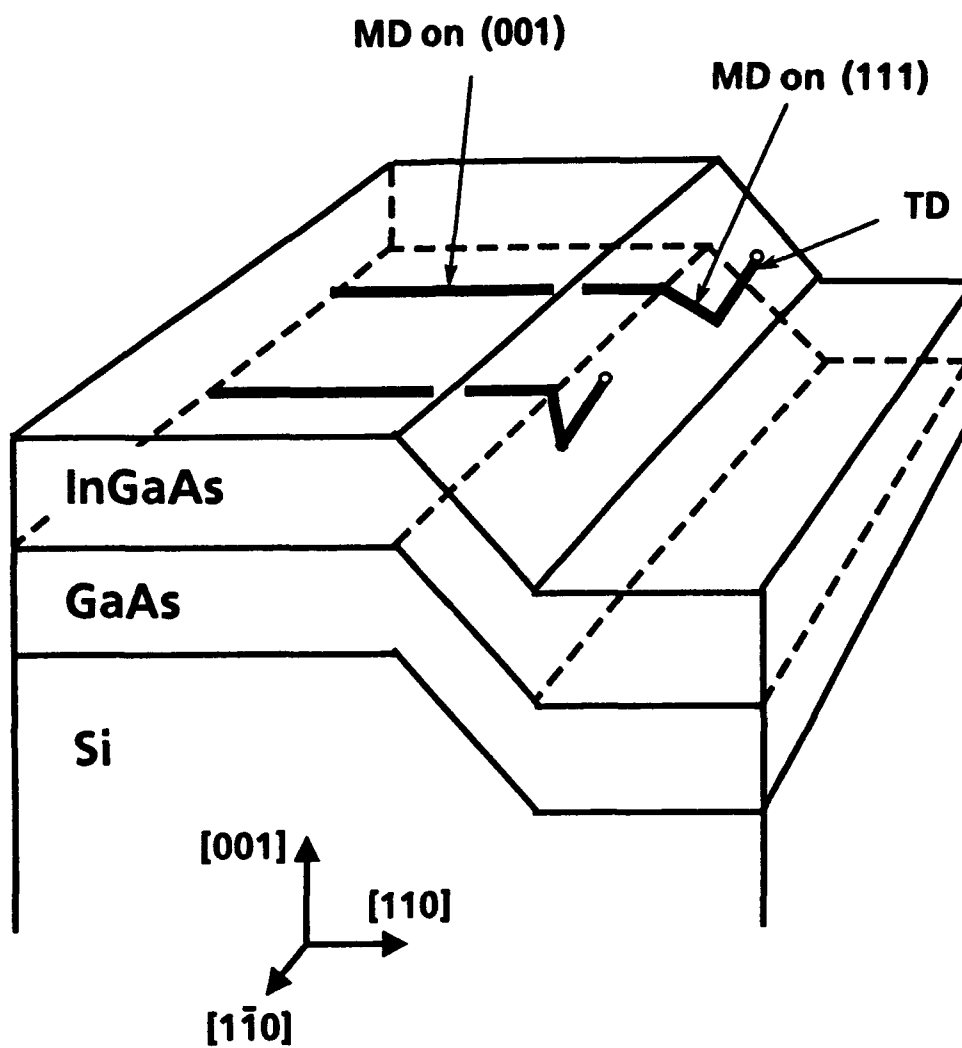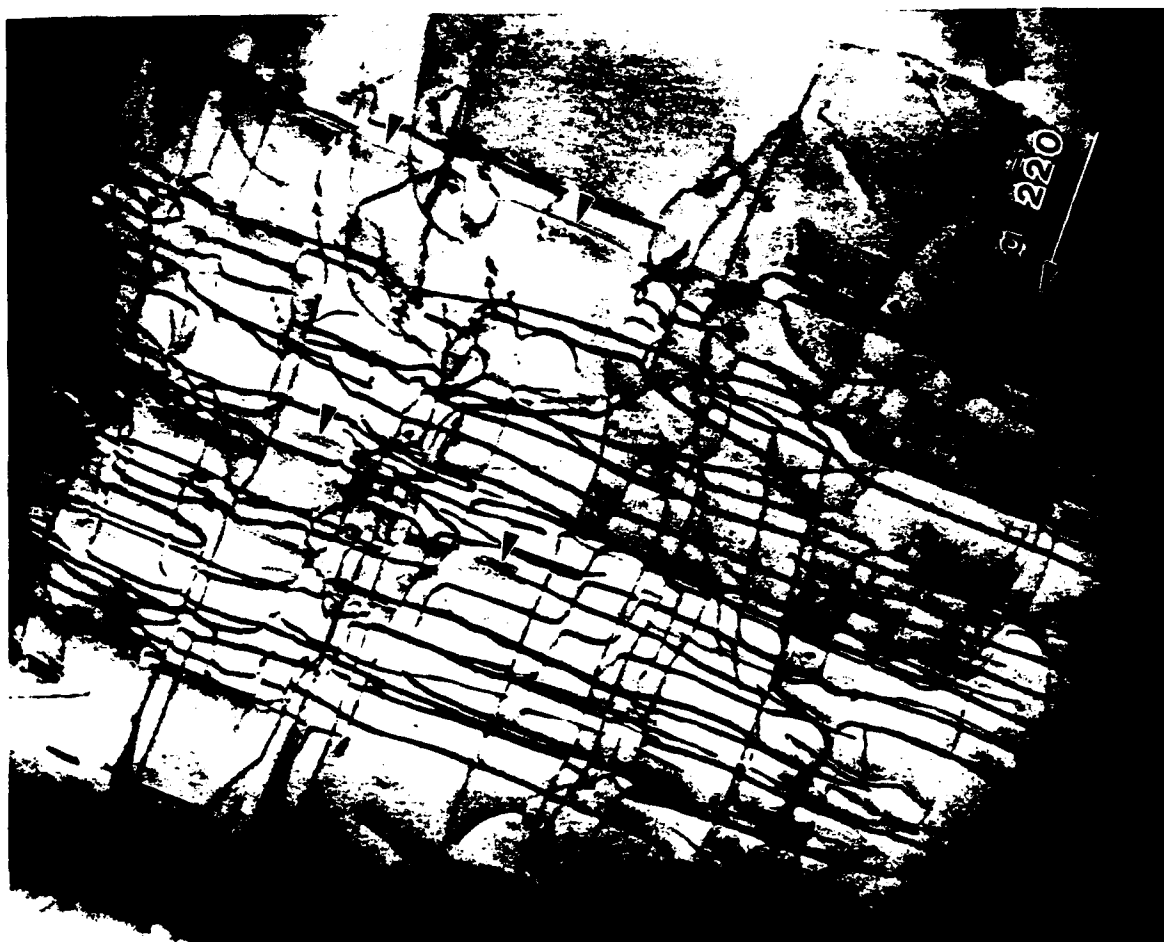
Table 1: Threading dislocation density, ρ_{TD} [10^7 cm^{-2}]

Film \\ Substrate	(A)	(B)	(C)	Pure GaAs (from ref. 2)
Concave sidewalls	13±4	12±4	30±15	70±30
{111} sidewalls	4±2	5±2		
Continuous	13±4	9±4	30±15	70±30

Atomic rearrangement at the interface of annealed ZnSe films grown on vicinal Si(001) substrates

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Significant atomic rearrangement at the interface was found to take place after post growth annealing treatments of epitaxial ZnSe on As passivated Si(001) substrates which were tilted by 4° towards the [1$\bar{1}$0] direction. The thermal stability of the ZnSe/As:Si interface was studied by rapid thermal annealing (RTA) at temperatures up to 960°C after growing an epitaxial GaAs cap layer to prevent evaporation of the ZnSe during the anneals. The ZnSe/As:Si interface was examined by high resolution electron microscopy (HREM). After an anneal at 900 °C the ZnSe/As:Si interface transformed from an atomically smooth interface found in the as grown films to a facetted structure with {111} oriented sidewalls that extended preferentially in the [1$\bar{1}$0] direction. The 60° dislocations that were previously observed along this direction combined into closely spaced pairs or into Lomer dislocations which were associated with the facets. We present a model for the atomic structure of the facetted interface which is consistent with the experimental data and satisfies electron counting considerations.

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I. INTRODUCTION

The chemical and structural stability of semiconductor interfaces is important in controlling device properties. For example, bandgap engineering relies on stable interfaces over only a few atomic layers.[1] In the case of heteroepitaxy on Si surfaces, the reactivity of the different components plays an important role. For GaAs on Si, the first As layer leads to a passivated surface and contributes to the island formation which dominates during the early stages of GaAs growth on Si. For ZnSe growth on Si, the reactivity of Se with the Si surface leads to formation of an amorphous $SiSe_2$ layer[2] and loss of epitaxy. In this latter case, a monolayer of As on the Si surface was found to have a positive effect, allowing uniform growth of ZnSe to occur[3]. In this paper we discuss another effect at heteroepitaxial interfaces, namely atomic rearrangement during post growth annealing. We will examine the stability of the interface formed when ZnSe is grown on the Si(100):As interface. After growth, this interface is flat on an atomic scale, but annealing at temperatures of around 900°C leads to a facetted interface in which the As atoms have stayed at the interface and the Si, Zn and Se atoms have diffused several nm.

ZnSe material systems are of current interest because of its application for blue laser diode devices[4]. Although most of the materials research has been reported for ZnSe films grown on GaAs since the lattice parameters are within 0.3%, growth of ZnSe on Si, is also of interest because of the potential for momolithic device integration with Si. ZnSe has a lower Knoop hardness than GaAs and has also been used as an interlayer between GaAs and Si substrates[5] in an attempt to lower the defect densities. In the annealing experiments carried out in this paper, it was observed that stacking faults in the GaAs overlayer were reduced after annealing of

the GaAs/ZnSe/Si combination. The effect of this annealing on the interface between the ZnSe and the Si substrate will be discussed in detail.

Rapid thermal annealing experiments were performed at temperatures up to 960 °C on ZnSe/Si films capped with an epitaxial GaAs overlayer. The ZnSe/Si interface was found to be stable during RTA temperatures up to 800 ° C. For RTA to 900°C, the interface became facetted and the misfit dislocation structure was rearranged. Above 950 °C pitting was observed in the film which was found by X-ray microanalysis to correspond to the loss of Zn. We present a mechanism for the formation of the facets as a result of the change in the dislocation structure and an atomic model of the facetted interface which satisfies electron counting criteria for low interfacial energy.

II. EXPERIMENTAL PROCEDURE

Films of ZnSe with a GaAs overlayer were grown by Molecular Beam Epitaxy (MBE) on arsenic terminated Si(001) substrates which were tilted by 4° towards the [1$\bar{1}$0] axis. Annealing of the clean vicinal Si(001) surface above 800°C before growth gives predominantly double-height steps with the Si-Si dimer direction and the step edges parallel to each other and to the [110] direction.(See the inset in figure 1a.) Addition of As to this surface at substrate temperatures below 400 °C results in a stable monolayer coverage of As-As dimers with the As-As dimer direction parallel to the [1$\bar{1}$0] direction. Arsenic termination of the Si(001) surface has been shown to allow the growth of continuous ZnSe layers without the reaction of Si and Se.[5] The ZnSe was grown at 300 °C and during growth of the GaAs overlayer the temperature was slowly ramped from 200 °C to 500 °C. Details of the growth procedure have been published previously.[3] The film thickness of each layer was about 20nm.

Reflection High Energy Electron Diffraction (RHEED) observations indicated that the growth mode of ZnSe on Si(001):As is two dimensional. The RHEED pattern shows evidence of surface roughness after growth of ~ 1.5 nm which gradually changes back to a complete two dimensional behavior for thicker films indicating a flat surface. This was confirmed by TEM which showed the film to be continuous at a thickness of 3 nm and to have a roughness of less than 1 nm at a thickness of 20 nm. This is in contrast to the similarly lattice mismatched case of GaAs on Si, where growth occurs by the nucleation and coalescence of large islands leading to rough surfaces.[6,7]

Rapid thermal annealing (RTA) experiments were carried out in a Heatpulse system using an ambient of N_2 for time periods of 20-45 seconds at temperatures ranging from 700 °C to 960 °C. The samples were sandwiched between two GaAs wafers and ramped to the peak temperature in a few seconds and then rapidly cooled to room temperature at about 80 °C/sec.

Crossectional TEM samples were prepared by cutting and polishing slices parallel to the ($1\bar{1}0$) and (110) planes before and after annealing. The polished samples were thinned to electron transparency on a liquid nitrogen cold stage using Ar ion milling at 4 keV. HREM images were taken at different values of defocus using a JEOL 3010 high resolution microscope at 300 kV. HREM simulations were performed of the images using the MacTempas multislice program[8] with values for the spherical aberration $C_s = 0.6$mm and a beam convergence angle $\alpha = 0.5$mrad.

III. RESULTS

Crossection HREM images of the ZnSe/Si interface with the e-beam parallel to the [110] and [$1\bar{1}0$] directions are shown in figures 1a-d. The overview images in figs. 1a and b show the Si substrate, the ZnSe film and the GaAs top layer. ZnSe has a

relatively low stacking fault energy and a large number of stacking faults are observed in the ZnSe layer in both projections. The ZnSe/Si interface is atomically abrupt and laterally smooth. A small broadening is observed at the interface when the e-beam is perpendicular to the step edges (see fig. 1b) due to the projection of 3-4 step edges within the thickness of the specimen. In the higher magnification images (fig. 1c,d) details of the dislocation structure are revealed. Only dislocations that extend perpendicular to the TEM specimen are visible for a given projection. The micrograph in figure 1c of a [110] projection shows three Lomer dislocations and one sixty degree dislocation along a 50 nm interface. The predominance of Lomer dislocations is characteristic of this projection and implies that a majority of the dislocations that extend parallel to the step edges are Lomer dislocations. On the other hand, images in the [1$\bar{1}$0] projection, i.e. when the step edges are parallel to the image plane, mainly 60° dislocations are observed. This is seen in fig.1d where only 60° dislocations are found along a 50 nm interface.

To probe the thermal stability of the interface, the samples were rapidly annealed to temperatures between 800 °C and 900 °C for 30 seconds. The interface remained sharp at an annealing temperature of 800 °C and then changed to a wavy appearance at 850 °C in both directions. Figure 2 is an image taken in the [110] projection which shows an undulating bright band at the interface. The stacking faults disappeared in the film but the misfit dislocation structure was unchanged, i.e. mainly 60° dislocations were observed to extend perpendicular to the step edges and mainly Lomers extended along the step edges.

Annealing at 900 °C resulted in a more substantial rearrangement of the interface. Facets with {111} orientated sidewalls have formed mainly in the [1$\bar{1}$0] projection. We interpret this as evidence of the formation of ridges that extend along the [1$\bar{1}$0] direction. A high density of ridges is observed at the interface when looking through a thick region of the sample as shown in figure 3a. The micrograph

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in figure 3b is from a thinner part of the interface which reveals ridges that are approximately 2 nm high and separated by about 85 nm. In figure 3c a higher magnification of individual facets shows that the misfit dislocation structure is associated with the facets. Before the anneal at 900 °C, the 60° dislocations that extended in the [1$\bar{1}$0] appeared separate and independent. After the anneal these 60° dislocations have combined into closely spaced pairs, where each pair is associated with a {111} facet (or ridge). No dislocations were found between the facets. Microchemical analysis of the interface revealed that the As interlayer remained at the ZnSe/Si interface after annealing up to 900 °C.

III. DISCUSSION

1. Energetics of Interface Formation

A model for the atomic arrangement of the ZnSe/As/Si(001) interface is shown in figure 4. Electron counting arguments show that this interface with Si-As-Zn-Se layers is locally neutral, whereas an interface formed of Si-Zn or Si-Se bonds is not[9]. This can be seen by considering that each Si atom contributes one electron per bond in bulk Si and each Zn (Se) contributes 1/2 (3/2) electrons per bond in bulk ZnSe. The number of electrons in bonds to the interface As layer is therefore 2 from the Si layer below, 2 x 1/2 from the ZnSe layer above and 5 arsenic valence electrons for a total of 8, satisfying the octet rule. There are two possible {111} interfaces but, because we know the orientation of the As-As dimers at the interface and the direction of the ZnSe crystal relative to the vicinal direction, we can eliminate one of the possibilities for the [1$\bar{1}$0] projection where the facetting is strongest. The (111) interface remaining has Se and As dimers parallel to the [1$\bar{1}$0] direction. A model for this interface which maintains the number of As atoms per unit area projected on the (001) face and also satisfies electron counting is shown in Fig. 4b.

HREM simulations were performed using these models for the (001) and (111) and an example is shown in figure 4c for the {111} interface. Strain was not included in the simulations and the value of the lattice parameter for ZnSe was set to be the same as that for Si. The simulation agrees quite well with the image (see fig. 3c) for a defocus of -10 nm and a thickness of 9.3 nm. This confirms our interpretation that the contrast difference in the image is due to facets.

2. Pseudopotential Calculations of the (100) and (111) ZnSe/As:Si Interfaces

To better understand the driving force for the formation of the {111} facets it is helpful to consider the relative energies of the dislocation-free {111} and (001) interfaces. If the interface energy for a {111} interface between ZnSe and As-terminated Si were significantly lower than that of the (001) interface, then very large {111} facets could form under equilbrium conditions. Facet formation will be energetically favorable if $\sqrt{3}\gamma_{111} < \gamma_{001}$, where γ_{111} is the interface energy for a {111} interface and γ_{001} is the energy for a (001) interface. The factor $\sqrt{3}$ arises from the fact that the contact area is increased by a factor of $\sqrt{3}$ upon (111) facetting.

Here we examine two possible structural models for the {111} interface and estimate the interface energies of these relative to a (001) interface in terms of a simple model of the energetics. The model assumes that one can separate the total energy into contributions from each atom and each bond. Formally we may express the total energy E as
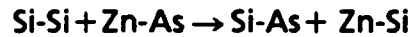
$$E - \Sigma n_i A_i = \Sigma n_{ij} B_{ij}$$

where A_i is the calculated energy of a single atom of type i and B_{ij} is the energy which we associate with a bond between atoms i and j. The n_i are the number of atoms of type i and the n_{ij} are the numbers of each type of bond. The B_{ij} are determined by fitting the results of pseudopotential total energy calculations[10] of

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$E - \Sigma n_i A_i$ for a set of structures .   By considering 12 different alloys containing various number of Zn, Se, Si and As atoms we were able to obtain a set of B_{ij} from which the total cohesive energies could be fitted to an accuracy of about 0.02 eV/bond. We consider only zincblende alloys having Si-Si, Si-As, Si-Zn, Si-Se, Zn-Se and Zn-As bonds and exclude those with Se-Se, Se-As, As-As or Zn-Zn bonds since these latter types of bonds are not present in the interface structures. With the six fitted values for the B_{ij} we may estimate the relative energies of the (001) and two types of {111} interfaces.

To determine the energy difference between the (001) and {111} interfaces, we must determine the difference in the bonding environments near the interface. As discussed in the caption of Fig. 5, the transformation from a (001) to a (111)B interface can be achieved through atom conserving reactions in which the bonding at the interface is changed according to the bond reaction:

$$Zn\text{-}Se + Si\text{-}As \rightarrow Zn\text{-}As + Si\text{-}Se.$$

A corresponding bond reaction

$$Si\text{-}Si + Zn\text{-}As \rightarrow Si\text{-}As + Zn\text{-}Si$$

leads to the formation of a (111)A interface. We may estimate the difference in energy ΔE between the facetted and (001) interfaces:

$$\Delta E = \sqrt{3} a^2 \gamma_{111} - a^2 \gamma_{001},$$

in terms of the bond energies. For the (111)B interface:

$$\Delta E_B = B_{Zn\text{-}Se} + B_{Si\text{-}As} - B_{Zn\text{-}As} - B_{Si\text{-}Se},$$

and for the (111)A interface:

$$\Delta E_A = B_{Si\text{-}Si} + B_{Zn\text{-}As} - B_{Si\text{-}As} - B_{Zn\text{-}Si}.$$

Within our model, $\Delta E_B = 0.46$ eV and $\Delta E_A = 0.55$ eV. It is also possible to calculate the *sum* $\Delta E_A + \Delta E_B$ from first principles by calculating the total energy for a

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supercell which contains both a (111)A and (111)B interface. In that calculation we find $\Delta E_A + \Delta E_B = 1.20$ eV. Thus the model is consistent with the first-principles calculation. From these results we conclude that the observed {111} facetting is inhibited by the change in chemical bonding. Instead it appears that facetting is driven by strain relief and interactions with the dislocations.

3. Strain Induced Facetting

The fact that the {111} facet leads to a higher interface energy than the (001) interface shows that it is not chemical energy alone that is causing the transition from a (001) interface to a facetted one. Some other effect, such as a reduction in strain energy by a change in the misfit dislocation structure must be invoked to explain the observed behavior. A change in the dislocation structure can lead to reduction in the energy associated with the strain fields that surround the dislocations. We will therefore examine the relationship between the facetting and misfit dislocations.

The difference in the dislocation type along the [1$\bar{1}$0] and [110] directions of the as-grown ZnSe/Si interface has been explained elsewhere[11] as being due to the presence of steps created by the 4° offcut of the Si substrate. Relaxation of misfit strain proceeds mainly by *glide* of threading segments associated with 60° misfit dislocations, and it was concluded that Lomer dislocations form by the combination of two 60° dislocations with appropriate Burgers vectors by this glide process. On a stepped (001) surface in the absence of any facetting, two 60° dislocations with matching Burgers vectors can propagate along the same line and form a Lomer segment if they propagate parallel to the step edges (in the [110] direction). However if they propagate perpendicular to the step edges (in the [1$\bar{1}$0] direction), they can not follow the same dislocation line and will form kinks at the steps in order to maintain continuity on the same glide plane. Lomer dislocations formed by glide

can occur in the [1$\bar{1}$0] for at most one terrace width. A [001] plan view schematic of the asymmetric dislocation structure for the non-facetted interface is shown in fig. 6.

Formation of a Lomer misfit dislocation from two parallel 60° misfit dislocations which preexist at the interface leads to a reduction of the total energy associated with the dangling bonds and the strain fields of the dislocations while the amount of misfit strain that is relieved remains unchanged. Hence there is an attractive force between 60° dislocations with matching Burgers vectors. Two such 60° dislocations can only approach each other by *climb* since they do not lie on the same glide plane. Annealing at high temperatures increases the dislocation climb mobility and therefore the ability of 60° dislocations to move along the interface towards one another. In the [1$\bar{1}$0] direction on a non-facetted (001) interface, the presence of steps produces kinks in a dislocation that tries to follow the interface. Kinks in the as-grown interface increases the dislocation line energy so a reduction in the number of kinks would also lower the total energy.

We suggest that the reduction in strain energy associated with the pairing of two 60° dislocations (parallel to the interface) and the reduction in the number of kinks in the dislocations provide the driving force for the formation of a facetted interface in the [1$\bar{1}$0] direction by atomic diffusion. Cooper͏ atomic diffusion takes place such that the amount of As at the interface is conserved and a {111} interface similar to that shown in Fig. 4b is formed in which all the atoms are fully coordinated and local neutrality is maintained. If the 60° dislocations combined completely at a facet, a Lomer dislocation would form that could travel continuously along one of the {111} oriented sides of the ridge as shown in fig. 7a. Although the [1$\bar{1}$0] TEM images reveal that the 60° dislocations do pair up at the facets, in most cases a Lomer did not completely form. (60° dislocations which were spaced by an average of 5 nm before annealing came together in pairs separated by less than 1 nm after annealing at 900 °C). The images indicate that in many cases one of the 60° dislocations in the pair

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travelled along the side of a ridge and the other remained near the stepped interface as illustrated in fig. 7b. This still leads to a significant reduction in the interface energy since the number of dislocation kinks is reduced and a closely spaced pair of 60° dislocations would have an energy approaching that of a Lomer.

The undulating interface found in the sample annealed at 850°C may indicate a pre-stage of facetting. The spacing of the 60° dislocations remains the same as in the unannealed sample and it appears that possibly a small amount of diffusion has taken place.

IV. CONCLUSIONS

A lower energy configuration for ZnSe grown on an arsenic terminated vicinal Si(001) surface was obtained by RTA at 900 °C. The reduction in strain energy associated with either the formation of closely spaced pairs of complimentary 60° dislocations or a Lomer dislocation supplied a driving force for atomic diffusion to form ridges at the interface which were parallel to the $[1\bar{1}0]$ direction and had {111} sidewalls. No dislocations were found between the ridges, and each ridge contained either a Lomer dislocation or a pair of 60° dislocations. The density of misfit dislocations corresponded to essentially a completely relaxed 4 % lattice mismatched interface.

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Figure 1: As grown HREM images in the a) [110] showing a smooth interface and stacking faults b) [1$\bar{1}$0] showing a broad interface. c) Higher magnification [110] showing Lomer dislocations (solid arrows), delocalized Lomer dislocation (open arrow) and a 60° dislocation (small black arrow). d) Higher magnification of [1$\bar{1}$0] showing only 60° dislocations. The inset in figure a) shows the convention used for labeling directions with respect to the stepped interface.

Figure 2:HREM image in the [1$\bar{1}$0] direction for a sample annealed at 850°C showing a wavy inteface with only 60° dislocations and no stacking faults.

Figure 3:HREM images in the [1$\bar{1}$0] direction for a sample annealed at 900°C. a) A thick region showing a high density of facets at the interface. b) A thin region showing well spaced facets. c) A higher magnification of three facets showing 60° dislocations (small arrow) and a Lomer dislocation (large arrow) in relation to the facets.

Figure 4: Atomic model of a) (001) and b) {111} faceted interface in [1$\bar{1}$0] for a ZnSe film on an arsenic terminated Si surface. c)HREM simulation of the {111} interface with value of the ZnSe lattice parameter the same as Si (i.e. no dislocations included).
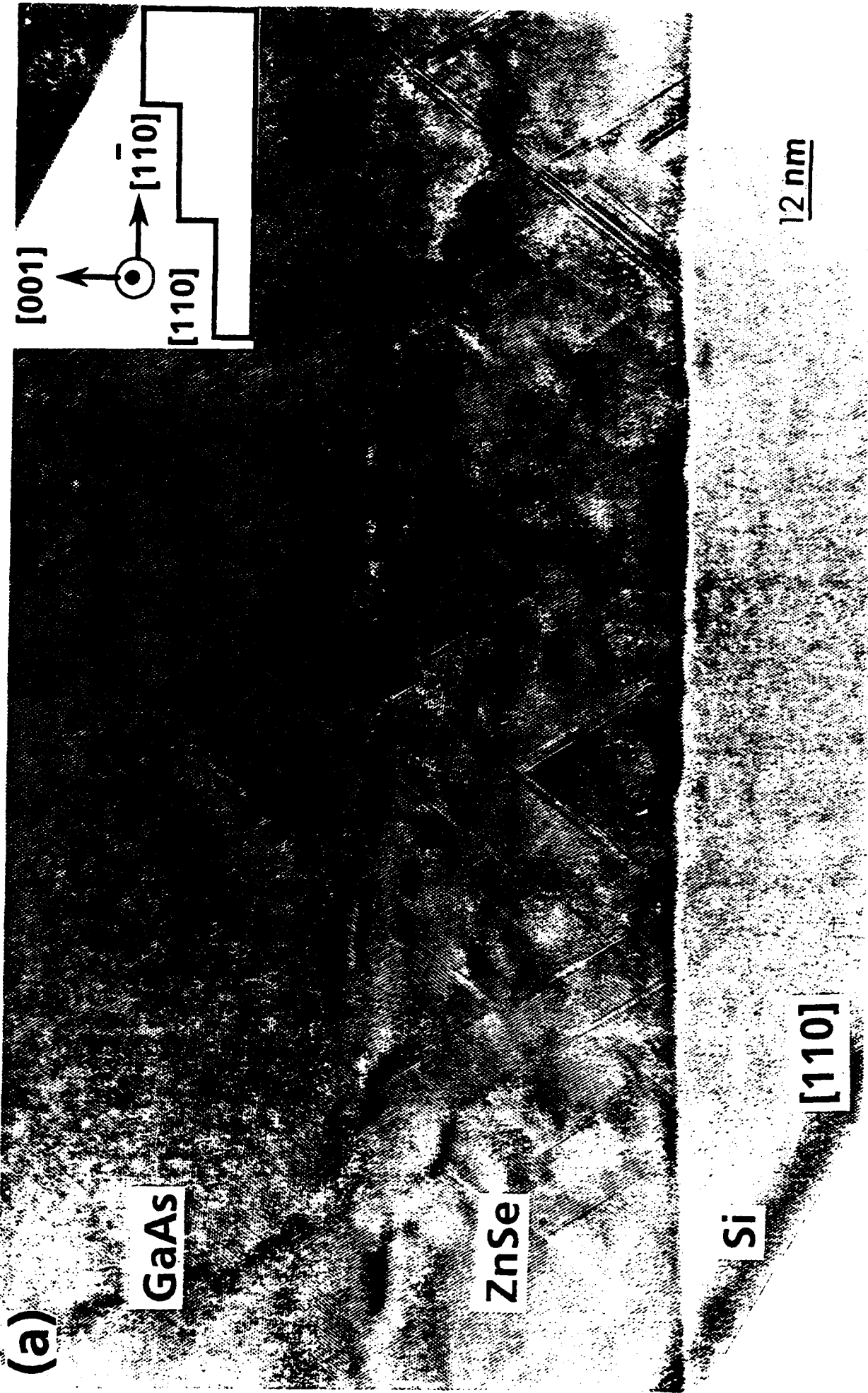
Figure 5: We define interface atoms as those with bonding environments different from the bulk. The atoms numbered 1-6 form a basis from which all the interface atoms may be obtained by appropriate translations. For the (111)B interface, shown in (a), the translation vectors are $R_1 = a[110] + \sqrt{2}a[001]$ and $R_2 = a[1\bar{1}0]$ where $a = 3.83$Å. The vector R_1 is indicated. All other atoms are in bulk-like bonding environments. In each unit cell (with an area $\sqrt{3}a^2$) there are 3 Si-Si bonds, 1 Si-As

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bond, 3 Zn-As bonds, 4 Zn-Se bonds, and 1 Si-Se bond associated with these six atoms. (b) Model for the (001) interface. Atoms near the interface are numbered 1-6. (Some of these six atoms are in bulk-like environments but are included to facilitate the comparison with the bonding in the (111)B interface.) Other interface atoms are obtained by translation of these six atoms along the vectors $R_1 = a[110]$ and $R_2 = a[1\bar{1}0]$. In each unit cell (which has an area equal to a^2) there are 3 Si-Si bonds, 2 Si-As bonds, 2 Zn-As bonds, and 5 Zn-Se bonds. In going from the (001) to the (111)B interface the net change in bonding corresponds to the reaction Zn-Se + Si-As $\rightarrow$ Si-Se + Zn-As.

Figure 6: [001] planview schematic of dislocations at the interface of an as-grown ZnSe film on a vicinal Si surface.

Figure 7:Schematic of terraced ZnSe/Si interface showing ridges with {111} sidewalls and either a) Lomer misfit dislocation or b) two 60° misfit dislocations.
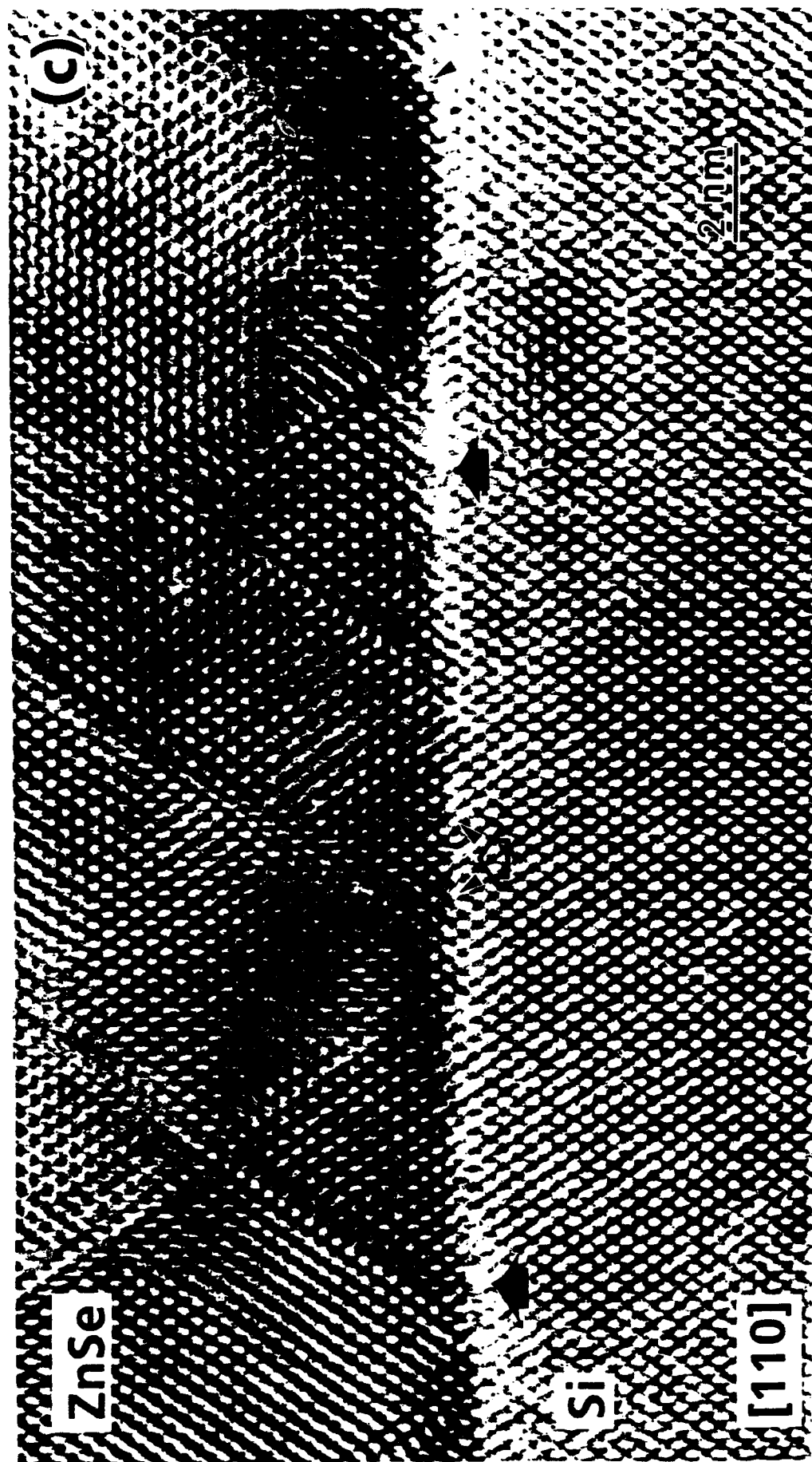
(a)

[001]
[110]
[1̄10]

GaAs

ZnSe

Si

[110]

12 nm

(b)
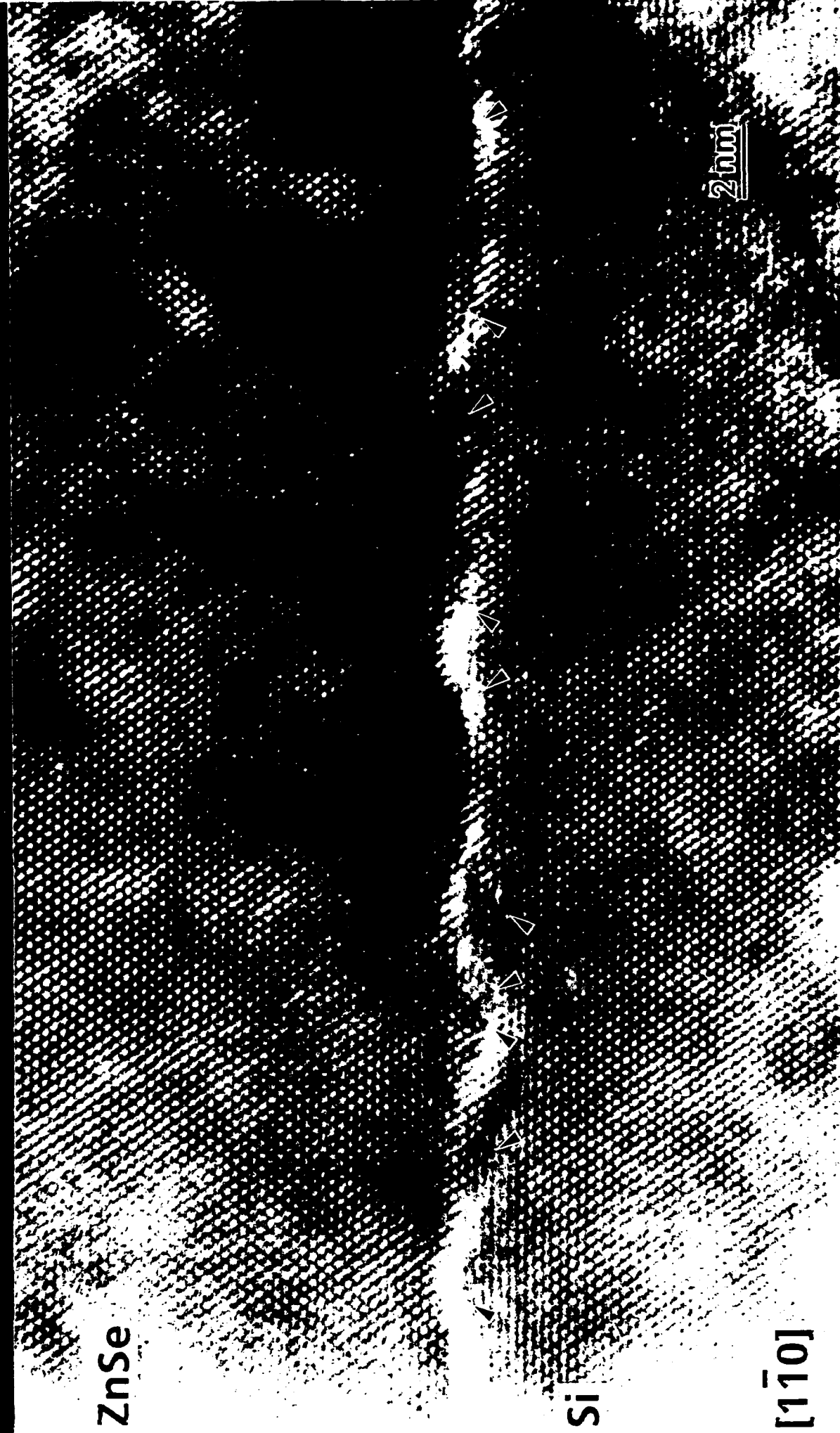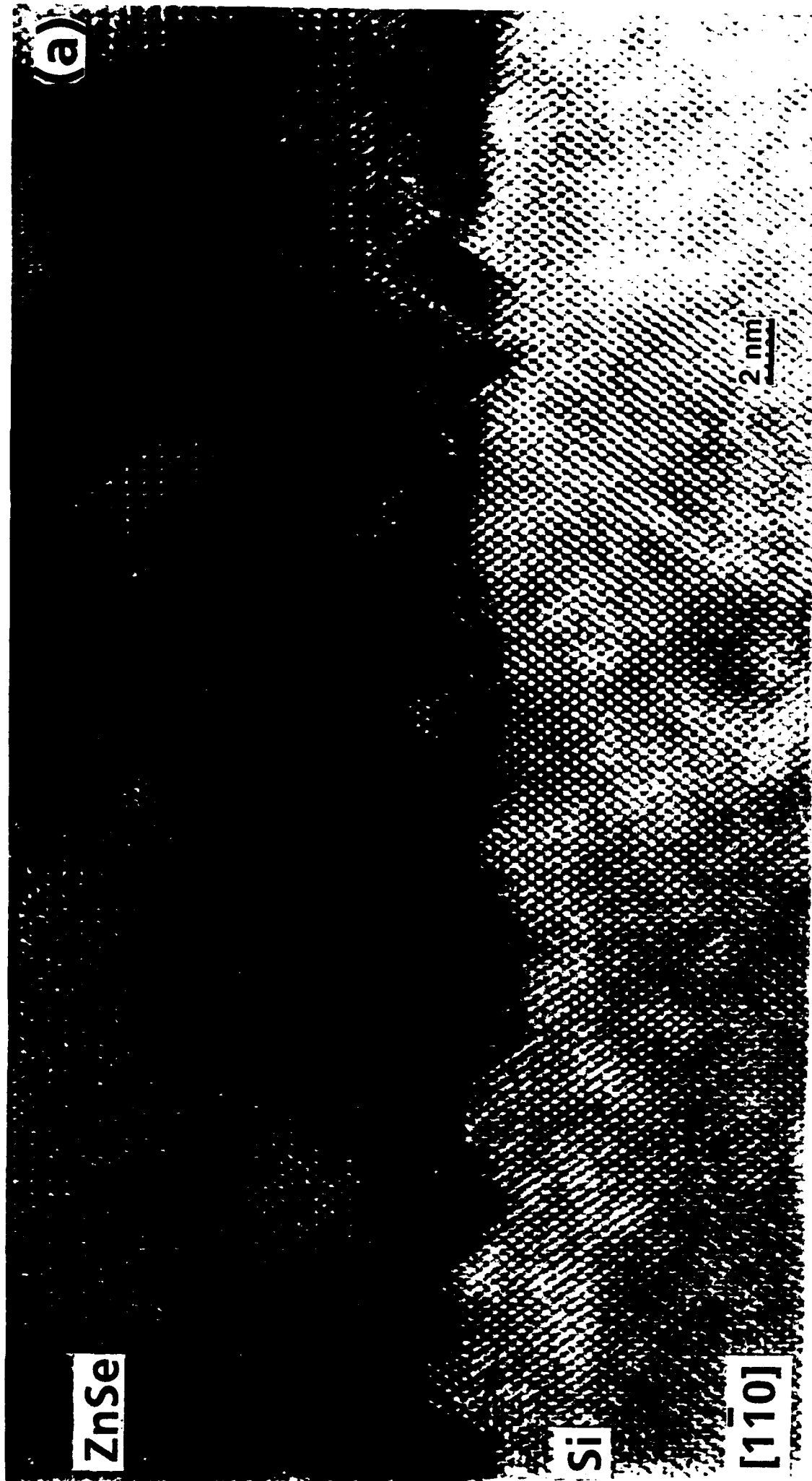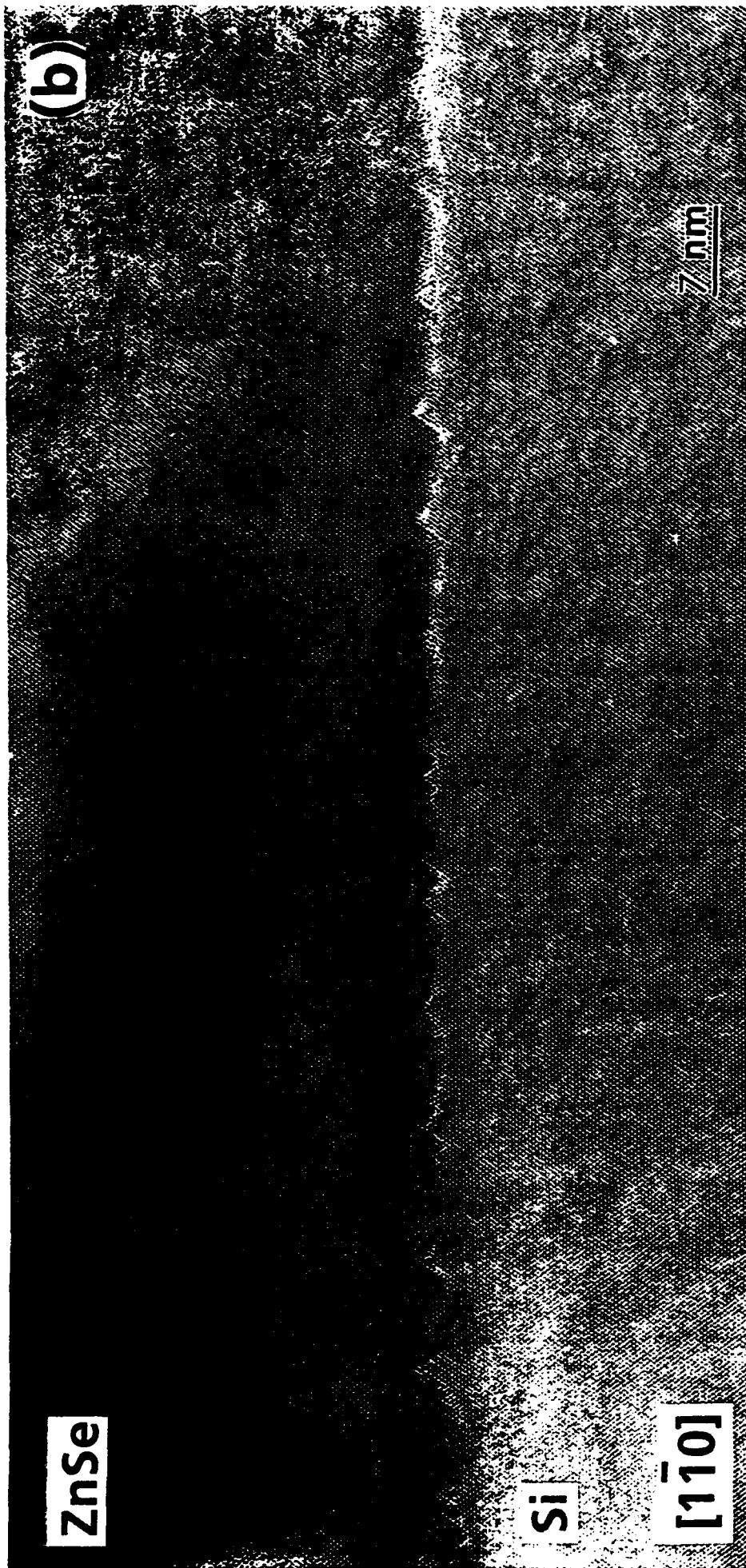
GaAs

ZnSe

Si

[$\bar{1}10$]

2 nm

(c) ZnSe / Si [110]

(d)

ZnSe

Si

2 nm

[1$\bar{1}$0]

850 °C RTA

ZnSe

Si

[1̄10]

2 nm

(a) ZnSe / Si [1̄10]

2 nm

(b)

ZnSe

Si

[1̄10]

7 nm

(c)

ZnSe

Si

[110]

2 nm

(a)

Se

Zn

As

Si

[001]

[110]

[1̄10]

(b)

2×4

Se

Zn

As

Si

[110]
[001]
[1̄10]
[110]

(a)

(b)

(111)B
Interface

[11$\bar{1}$]

[001]

[110]

[$\bar{1}$10]

1 2 3 4 5 6

Se

Zn

As

Si

Fig. 5

[1̄10]

Si

ZnSe

As

(c)

Fig. 5

Lomer dislocation

60° dislocation

Step edge

[1̄10]

[110]

[001]

Fig. 6

(a)

{111} Ridge

Lomer

ZnSe

Si

[001]

[1$\bar{1}$0]

[110]

(b)

60° dislocations

ZnSe

Si

Fig 7
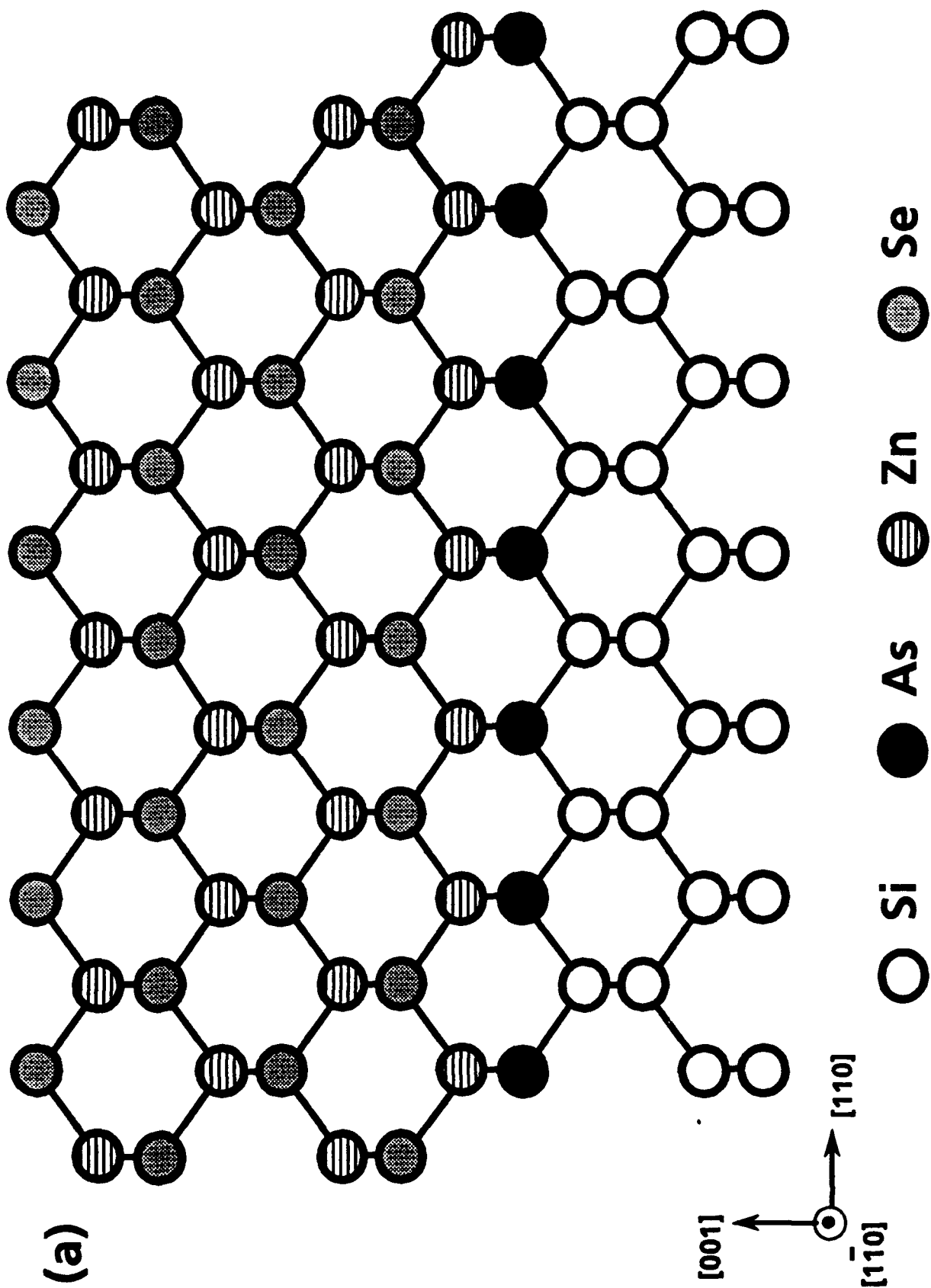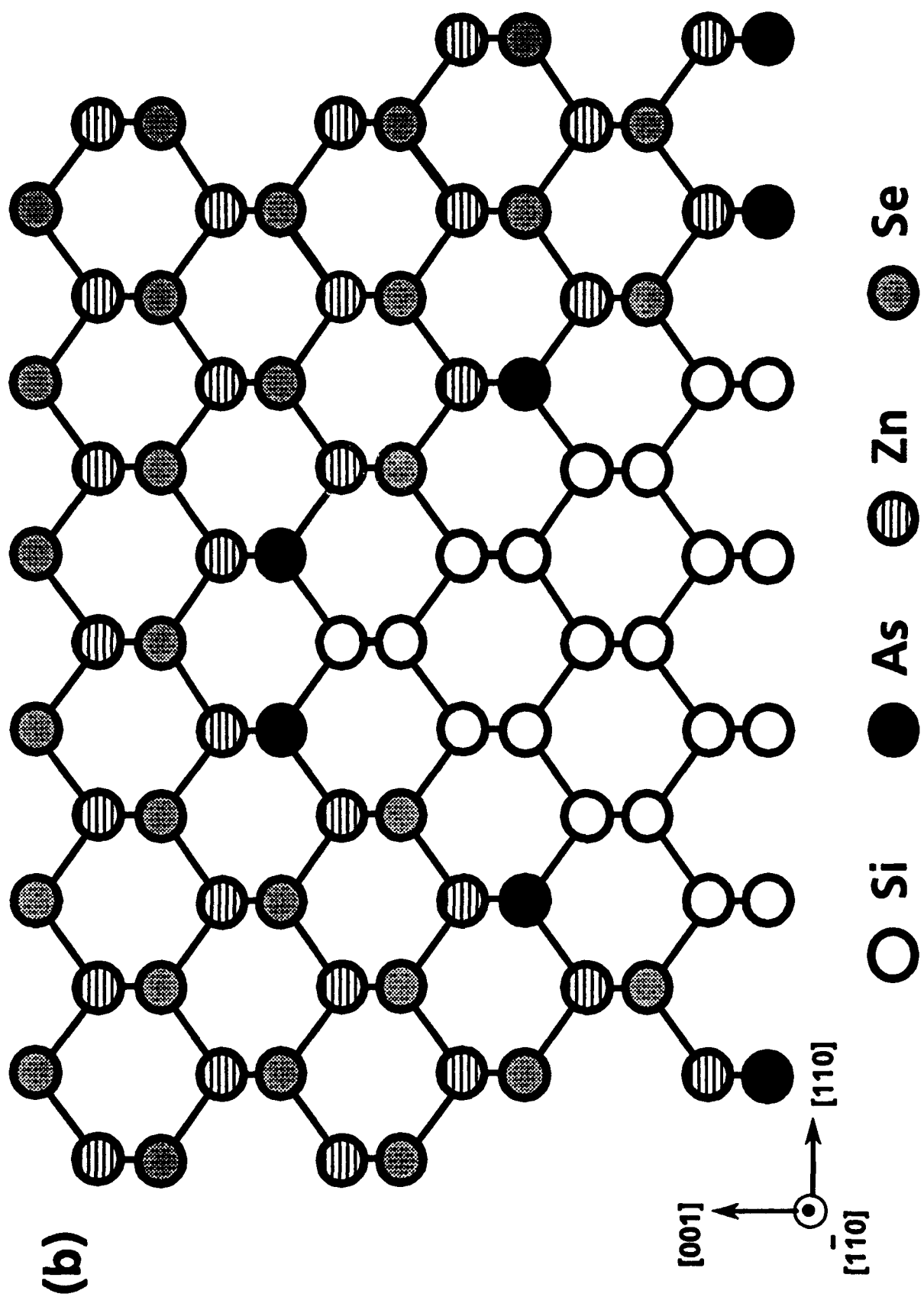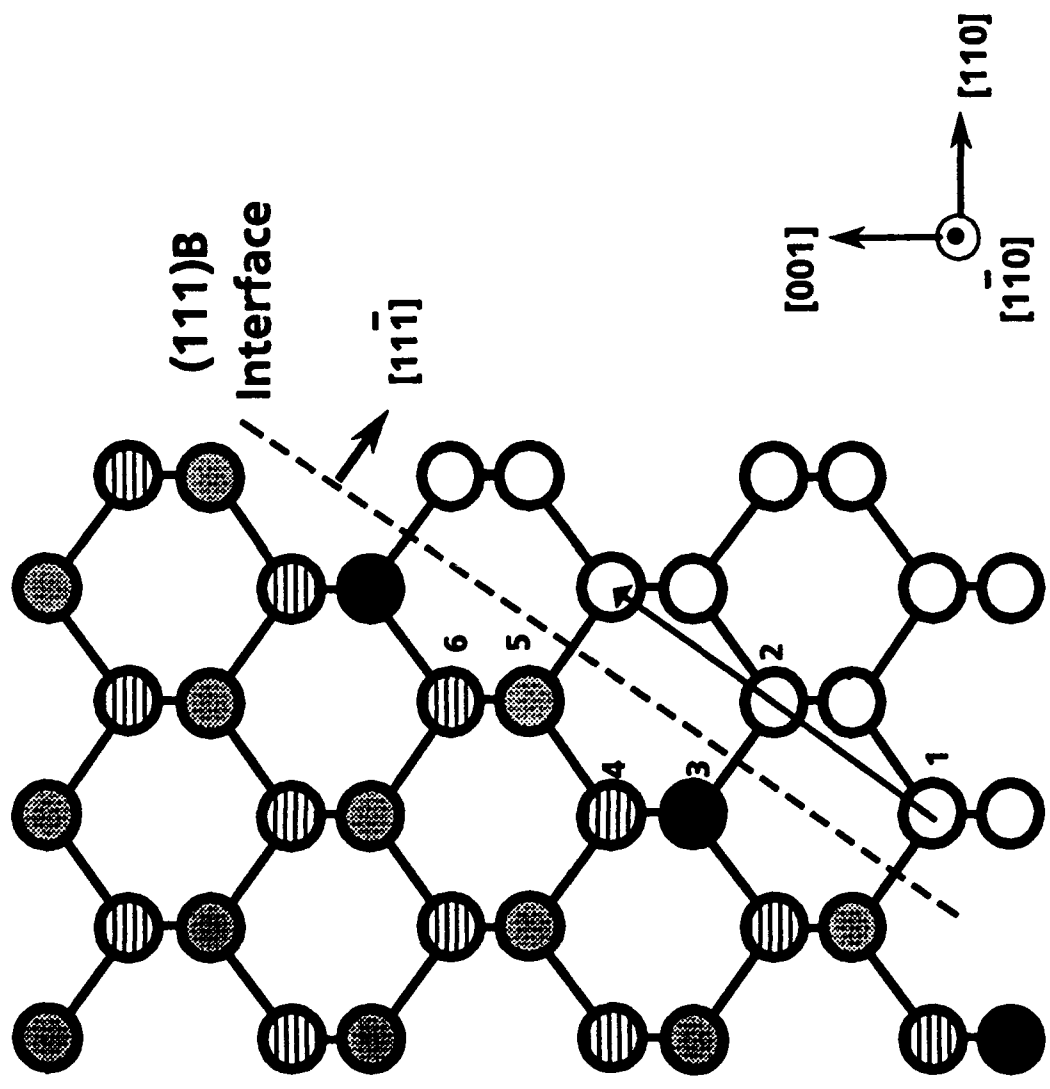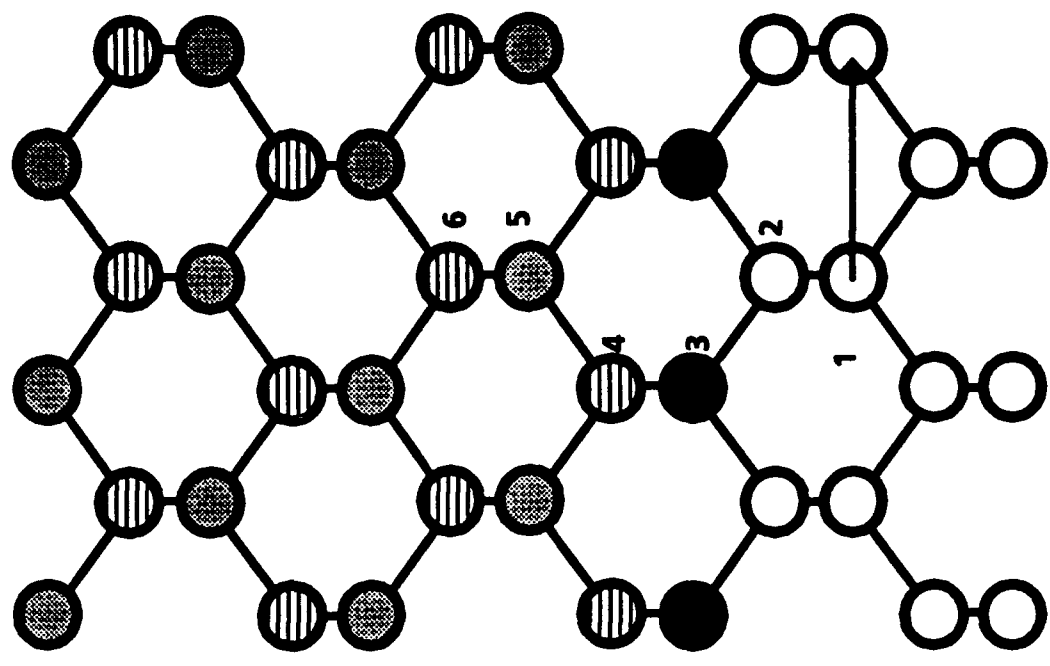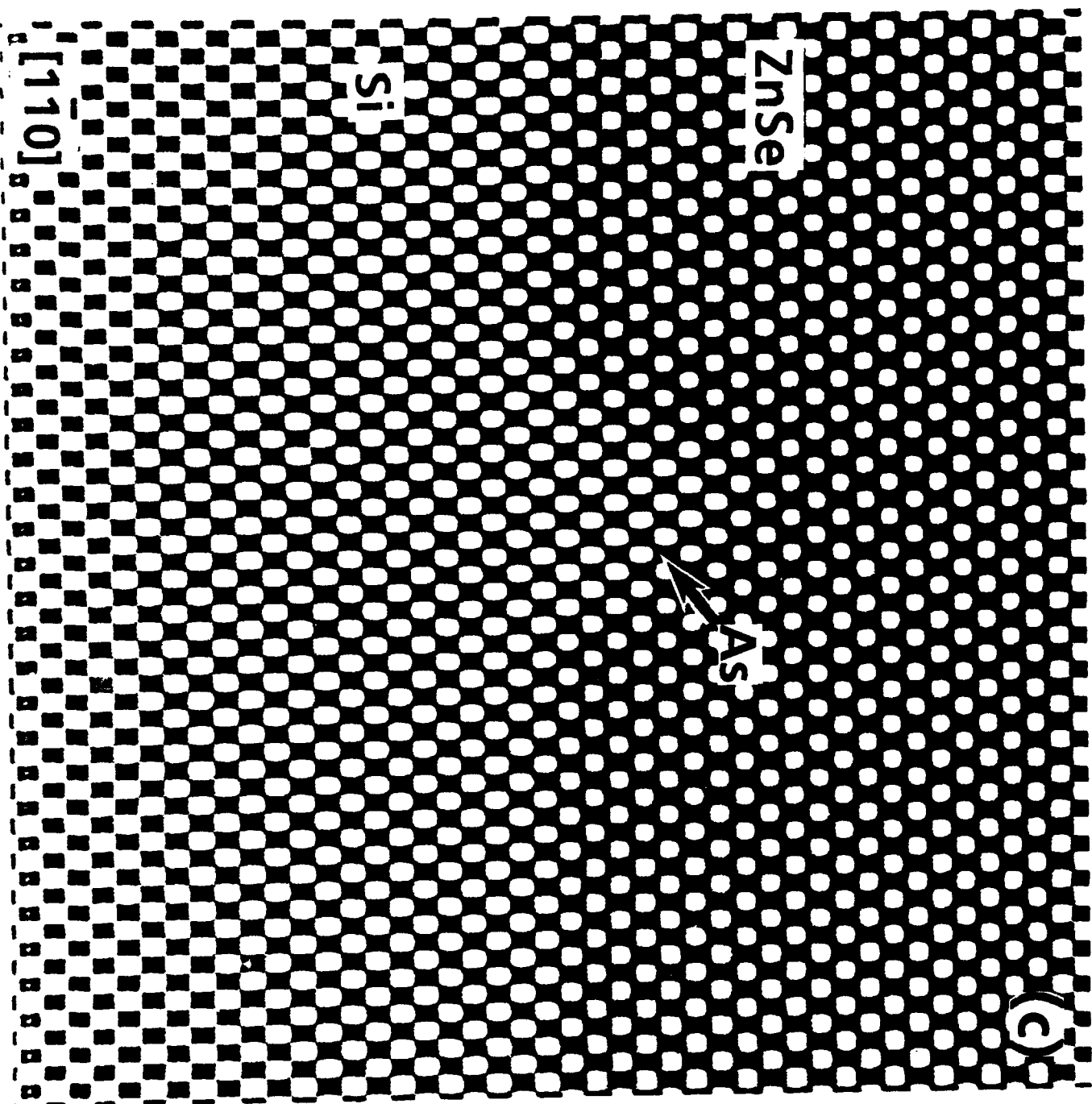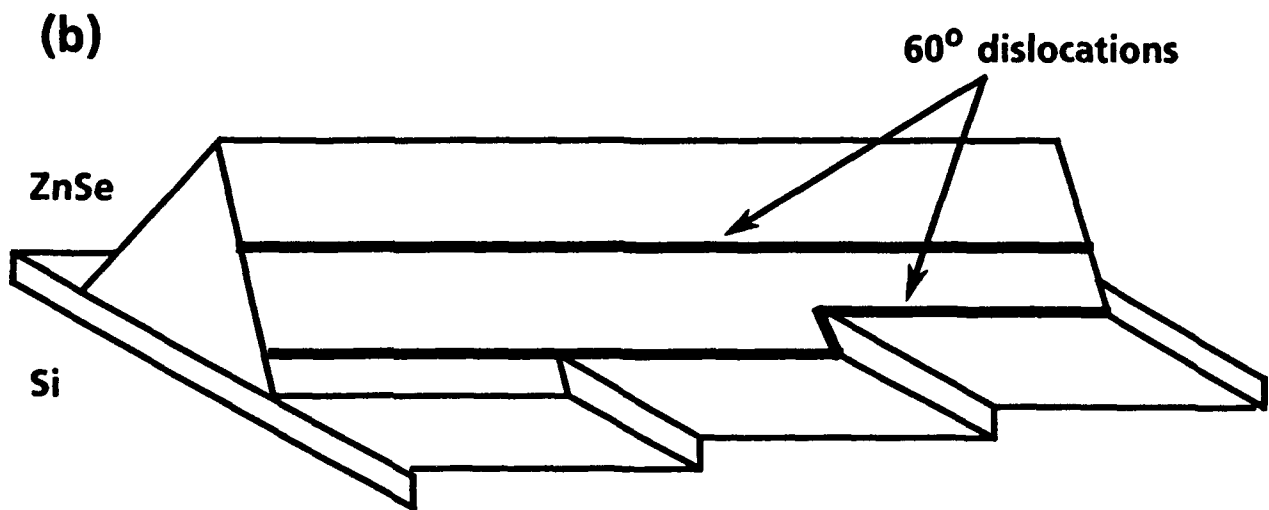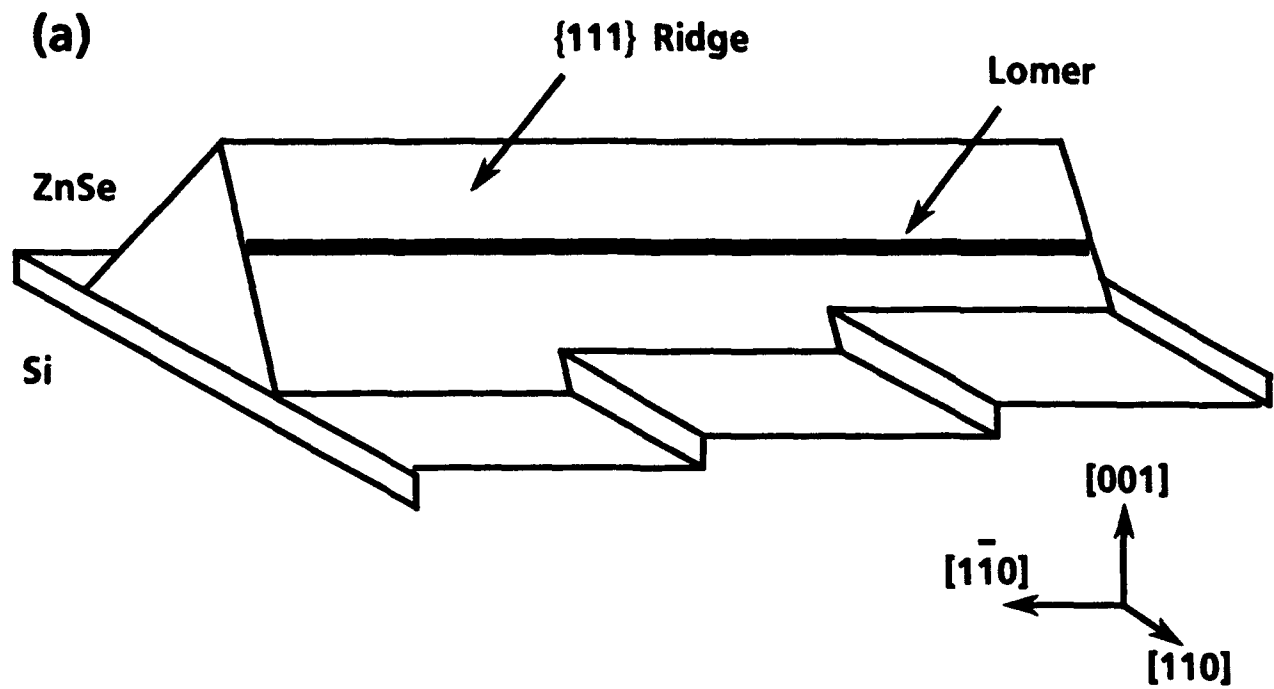
Misfit Dislocations in ZnSe Grown on Vicinal Si (001) Substrates

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Abstract

High resolution electron microscopy (HREM) has been used to study misfit dislocations of ZnSe films grown on vicinal Si (001) substrates tilted 4° towards the [1$\bar{1}$0] axis. In images taken with the electron beam parallel to the [1$\bar{1}$0] direction, 60° dislocations were found to predominate whereas mostly Lomer dislocations or closely spaced 60° dislocations (separa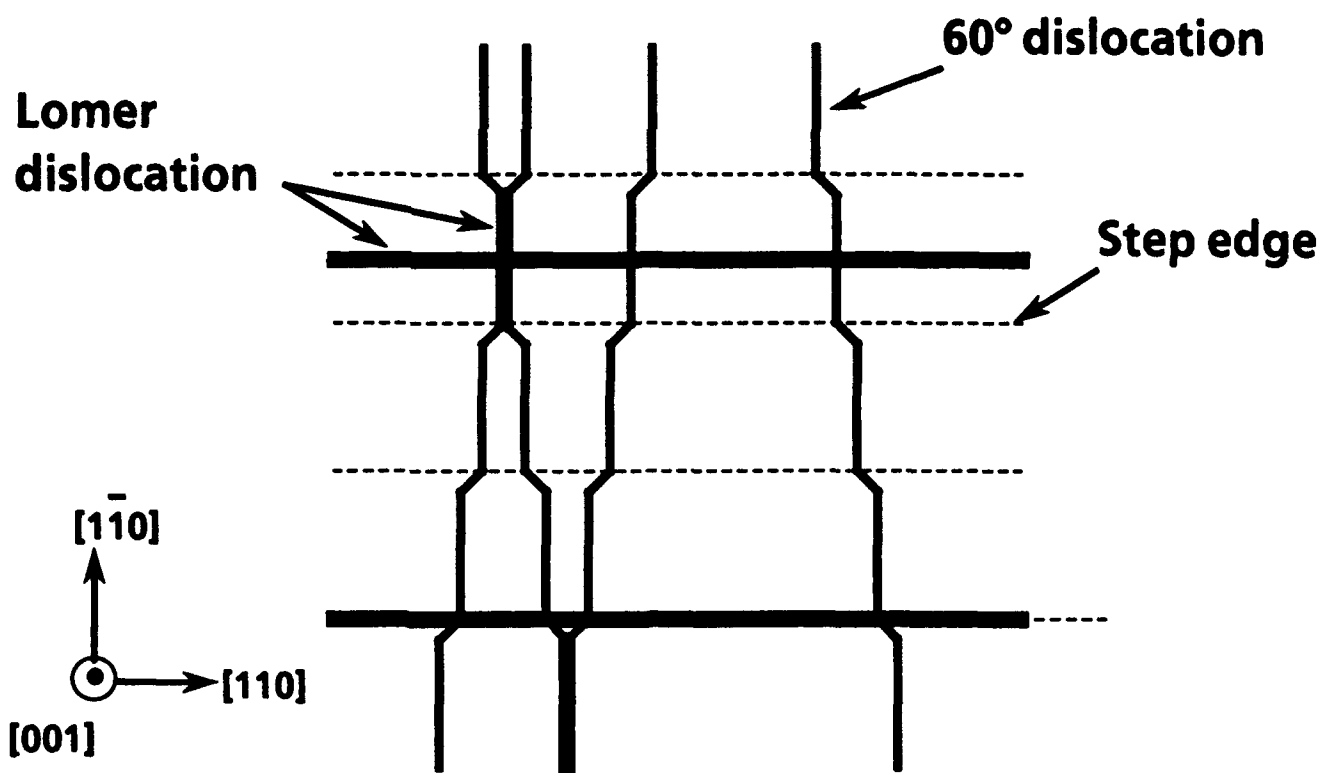ted by < 2nm) were observed in images taken in the orthogonal direction. A model is presented here to explain the formation of the asymmetric dislocation structure on the basis of mechanisms for propagation and formation of misfit dislocations.

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ZnSe is presently of major interest for blue light-emitting optical devices. Laser diodes have been fabricated in ZnSe-based material grown on lattice matched GaAs substrates.[1,2] However the growth of ZnSe on Si substrates [3,4] would allow for the technologically important monolithic integration of ZnSe devices with silicon integrated circuits. ZnSe is also plastically and elastically much softer than GaAs and has been investigated as an interlayer to lower the residual strain and defect density in GaAs grown on Si.[5-7] The 4% lattice parameter difference for ZnSe on Si makes this system one of a large group of technologically important lattice mismatched heteroepitaxial systems. For all of these systems control of the defect structure is essential for the success of devices. Since film defects are closely related to the misfit relieving dislocations at the interface it is important to build an increased understanding of the processes that determine the interface defect structure.

In this letter we report on a study of the interface dislocation structure of ZnSe grown on vicinal Si (001) substrates. The use of vicinal substrates was found by Fischer et al to reduce threading dislocation densities in GaAs grown on Si.[8] They postulated that Lomer dislocations would form at step edges and used Si substrates with the (001) surface tilted 4° towards [1$\bar{1}$0] to allow for a sufficient number of steps to be created. (The convention for labeling of directions in this paper is shown in Fig. 1). The decrease in dislocation density was attributed to the efficiency of Lomer dislocations in relieving interfacial strain since their Burgers vectors lie parallel to the interface plane. However Tsai and Kao later suggested that growth on tilted substrates would form threading dislocations with Burgers vectors that would tend to annihilate as the film grows.[9] In addition, cross section high resolution electron microscopy (HREM) showed that predominately Lomer dislocations extend in the direction parallel to the step edges ([110] direction) and 60° dislocations exter.u perpendicular to the step edges ([1$\bar{1}$0] direction).[8]

In the present study of ZnSe on vicinal Si(100) substrates we have made a similar observation that Lomer misfit dislocations predominate perpendicular to the tilt axis and 60° dislocations predominate in the orthogonal direction. A new mechanism is proposed which explains this result in terms of the propagation and interaction of misfit dislocations during growth and plastic relaxation of the epitaxial film. We conclude that steps do not directly lead to the formation of Lomer dislocations but instead hinder their formation in the [$1\bar{1}0$] direction.

ZnSe films were grown at 300° C by Molecular Beam Epitaxy (MBE) on arsenic terminated Si(001) substrates which were tilted by 4° towards the [$1\bar{1}0$] axis. Appropriate annealing of the Si(001) surface gives predominantly double-height steps and termination of this surface with a monolayer of arsenic has been shown to allow the growth of continuous ZnSe layers without the reaction of Si and Se.[5] Details of the growth procedure have been published previously.[10] Crossectional HREM samples were prepared by cutting and polishing slices parallel to the ($1\bar{1}0$) and (110) planes. The polished samples were thinned from both sides using Ar ion milling at 4 keV and a liquid nitrogen cold stage. The TEM images were obtained in a JEOL 3010 high resolution microscope at 300 kV.

Reflection High Energy Electron Diffraction (RHEED) observations indicated that the growth mode of ZnSe on Si is two dimensional. The RHEED pattern shows evidence of surface roughness after growth of ~ 1.5nm which gradually changes back to a complete 2D pattern for thicker films indicating a flat surface. This was confirmed by TEM which showed the film to be continuous at a thickness of 3nm and to have a roughness of less than 1nm at a thickness of 20nm. This is different from the case of GaAs on Si which grows by the nucleation of large islands leading to very rough surfaces.[11,12]

Figures 2(a) and (b) are HREM images of the ZnSe/Si interface in the [110] and [1$\bar{1}$0] directions respectively (i.e. with the electron beam parallel to the [110] and [1$\bar{1}$0] directions respectively). In figure 2(a) the (001) lattice planes are at a 4° tilt relative to the interface. Two Lomer misfit dislocations with localized dislocation cores, a dissociated Lomer misfit with a delocalized core separated by three (111) planes, one 60° misfit dislocation and several stacking faults are observed in this region. The ratio of Lomers (with localized and delocalized dislocation cores) to 60° dislocations was about 4:1 along a 200nm length of the interface containing about 15 dislocations. We did not observe any correlation between step edges and Lomer dislocations.

In figure 2(b) the (001) lattice planes are parallel to the interface. One delocalized Lomer misfit dislocation, five 60° misfit dislocations and several stacking faults are observed along this region. There were approximately 20% fewer stacking faults found along this interface compared to the [110] orientation. The ratio of Lomer to 60° dislocations along a 200nm interface was about 1:4. Furthermore a correlation between neighboring 60° dislocations was observed along this direction. The component of the Burgers vector that is perpendicular to the interface was generally found to have opposite signs on neighboring dislocations.

In order to understand the predominance of 90° misfit dislocations along [110] and of 60° misfit dislocations along [1$\bar{1}$0], it is necessary to look at how the dislocation network is built up during growth and during plastic relaxation of the film. The mechanism for nucleation of misfit dislocations in heteroepitaxial systems with 2-5 % lattice mismatch has been extensively debated in the research literature over the past 20 years. A number of nucleation mechanisms have been suggested.[13-16] Regardless of the mechanism for dislocation nucleation, it is clear

that a major process responsible for relaxation is the extension of misfit dislocation segments along the interface. In the case of a 60° dislocation, propagation can occur through glide of the associated threading segments on <111> planes. However for a Lomer misfit dislocation to extend in length, its associated threading segments would have to climb. The process of climb is a diffusion limited process and therefore inherently much slower than glide. At the growth temperatures typically used, climb of dislocations should not play a significant role in formation of the dislocation structure. This leads to the question of how the observed extended Lomer dislocations are formed. Previously it has been suggested that steps in the substrate surface or island coalescense are involved in the formation of Lomer dislocations[8,17] or that a small amount of climb would occur to combine two parallel 60° misfit dislocations that have Burgers vectors (b) which add to form a 90° dislocation in the interface plane.[18] More recently it has been suggested that this combination of 60° misfit dislocations can also occur without climb, by the nucleation of a complementary 60° dislocation directly at the site of a pre-existing 60° dislocation at the interface.[19,20] This nucleation mechanism has also been supported by theoretical calculations.[21] The complementary dislocation is nucleated in the form of a loop in which the upper segment leaves the film at the free surface. These threading segments would then glide to extend the new misfit dislocation along the pre-existing dislocation, producing an extended 90° dislocation.

In addition to these mechanisms we suggest that Lomer dislocations can form through glide of threading segments without the nucleation of a new dislocation. A complementary 60° dislocation can meet a pre-existing 60° dislocation, without climb, if the two dislocations initially extend along perpendicular directions. An example illustrating this situation is shown in the [001] plan view diagram in figure 3. This example considers two initially orthogonal misfit dislocations (A) and (B) on

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an on-axis (001) oriented interface. Misfit dislocation (A) with $\underline{b}= a/2[01\bar{1}]$ has a [$\bar{1}$10] line direction [with its threading dislocation on the (111) plane] and misfit dislocation (B) with $\underline{b}=a/2[101]$ propagates along its [110] line direction towards dislocation (A) by glide of its threading segment on the ($1\bar{1}\bar{1}$) plane [see fig. 3(a)]. When dislocation (B) intersects dislocation (A) its threading segment can switch glide plane to the ($\bar{1}\bar{1}1$) plane and start to glide along the line direction of dislocation (A) [see fig. 3(b)]. A Lomer misfit segment is formed that is a combination of (A) and (B) with $\underline{b}=a/2[110]$. The formation of a Lomer dislocation from two 60° dislocations is energetically favorable since a Lomer dislocation relieves the same amount of stress while the the total energy associated with the dislocation cores will be reduced. This type of interaction has a high probability since statistically 1/4 of all intersections will occur between 60° misfit dislocations with matching Burgers vectors that add up to form the appropriate $\underline{b}$ for a Lomer dislocation.[22]

The picture of forming a Lomer dislocation by the propagation of a complementary 60° misfit along a pre-existing 60° misfit assumed a flat (001) interface. This will now be refined for our case of a stepped interface. Each of the schematic drawings in figures 4(a)-(c) depicts the terraced interface between Si and the ZnSe and the glide planes of two matching 60° misfit dislocations. Two 60° misfit dislocations that can form a Lomer have threading segments gliding on different <111>planes. It is clear from figure 4(a) that for misfit dislocations extending parallel to the step edges the two glide planes can intersect the interface along the same line for long distances, and it is possible for complimentary 60° dislocations to propagate along this line to form an extended Lomer. However, in the [$1\bar{1}0$] direction, dislocations would have to switch glide planes at the steps in order to maintain the *same* line at the interface. This would result in a jog for both the misfit and the threading segment of each dislocation [figure 4(b)]. Jog formation involves

dislocation climb and hence there are strong kinetic arguments that favor formation of the following structures. As a threading segment passes over a step it would be kinetically much easier to retain the entire dislocation on the same glide plane and only insert a kink in the misfit segment as illustrated in figure 4(c). This implies that the dislocation lines of the two 60° misfit dislocations will shift laterally and in opposite directions along each step. This means that a complementary 60° misfit dislocation (C) can not follow a pre-existing misfit (D) for more than one terrace width. It also means that parallel 60° dislocations are able to come together as they traverse steps and can form Lomers, but only with lengths equal to a terrace width. The schematic structures shown in Figs. 4(a) and 4(c) are consistent with our observation of predominantly Lomer dislocations in the [110] direction and randomly spaced 60° misfit dislocations parallel to the [1$\bar{1}$0] direction, respectively.

The GaAs/Si interface exhibits the same asymmetry in the dislocation structure[8] as we have observed for the ZnSe/Si interface. In view of this similarity we suggest that the same mechanism for the formation of Lomer dislocations prevails in both cases. This contradicts the supposition that the lower dislocation density in GaAs films grown on vicinal Si(001) substrates compared to on-axis (001) surfaces arises because the step edges act as preferential nucleation sites for Lomer dislocations which would not thread through the film.[8] To the contrary it indicates that the surface steps suppress formation of Lomers in the [1$\bar{1}$0] direction, and it has since been shown that the formation of Lomers is detrimental for achieving low threading dislocation densities.[7] In the present work it was found that misfit dislocations are not preferentially located at steps. For the growth of GaAs on Si the situation is ambiguous since a correlation between step edges and Lomer dislocations has been reported in earlier[17] but not later cases.[9,23] However, Lomer formation by glide of threading segments does not exclude the possibility of a correlation between step

edges and Lomer dislocations since it is conceivable that step edges could act as preferential nucleation sites for the "pre-existing 60° misfit dislocation".

In conclusion, a model has been presented to explain the observation of predominately 60° misfit dislocations oriented perpendicular to the step edges and predominately Lomer dislocations oriented parallel to the step edges on 4° misoriented ZnSe/Si interfaces. The model describes the propagation of misfit dislocations along stepped and flat interfaces. It is based on the glide of threading segments of 60° misfit dislocations for the formation of Lomer dislocations. This model can also explain the same observation found at the interface for similar systems such as GaAs films grown on vicinal Si(001) substrates even though the initial nucleation stages are different.

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FIGURE CAPTIONS

Figure 1. Sign convention used for the relationship between the stepped Si surface and the ZnSe film direction.

Figure 2. HREM images of a ZnSe film deposited on an arsenic terminated, vicinal Si(001) surface at 300°C. (a) The image is taken with the beam parallel to [110] direction showing 60° dislocations (small black arrows), Lomer dislocations (large solid arrows), and a dissociated Lomer disslocation (open arrow) composed of two 60° dislocations. (b) The image is taken along the [1$\bar{1}$0] direction showing 60° dislocations marked by black arrows.

Figure 3. Schematic [001] plan view of the interface showing (a) the interaction of a propagating 60° misfit dislocation "B" by glide of its threading segments (dotted lines) with a pre-existing 60° misfit dislocation "A". This reaction forms (b) a 90° Lomer dislocation that has the same line direction as "A". (A 3-dimensional view of misfit segments and corresponding threading segments on <111> planes is illustrated in figure 4)

Figure 4. Propagation of misfit dislocations and their associated threading segments on <111> glide planes along the interface. In (a) the misfit dislocation is continuous on the terrace of a stepped interface. In (b) the misfit dislocation extending perpendicular to the step edges must form jogs at the steps for it to maintain the *same* line at the interface Alternatively as shown in (c), a 60° misfit dislocation can form kinks at the step edges to allow its threading segment to remain on the same glide plane or a Lomer dislocation is forced to separate into two 60° dislocations "C" and "D" as described in the text.

ZnSe

[001]

$[\bar{1}10]$ ←

→ [110]

Si

Fig. 1.

(a)

ZnSe

Si

2 nm

[110]

(b)

ZnSe

Si

2nm

[1̄10]

(a)

$\underline{b}_A = a/2[01\bar{1}]$

60° MD "A"

60° MD "B"

$\underline{b}_B = a/2[101]$

(b)

$\underline{b}_{AB} = a/2[110]$

90° MD

[010]   [100]

[001]

(a)

[001]
[1̄10]
[110]

Glide plane

ZnSe

Si

Lomer   60° misfit   Threading dislocation

(b)

(c)

"C"

"D"

Lomer